TJA1463

CAN FD signal improvement transceiver with Sleep mode

Rev. 3.0 — 12 February 2025

Product data sheet

1 General description

The TJA1463 is a member of the TJA146x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA146x transceivers implement the CAN physical layer as defined in ISO 11898-2:2024 third edition and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers.

The TJA1463 includes CAN signal improvement capability (SIC), as defined in ISO 11898-2:2024 parameter set C. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in larger topologies. In addition, the TJA1463 features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8 Mbit/s.

The TJA1463 is intended as a simple replacement for high-speed Classical CAN and CAN FD transceivers, such as the TJA1043 and TJA1443 from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJA1463 to be easily retrofitted to existing applications.

An AEC-Q100 Grade 0 variant, the TJR1463, is available for high temperature applications, supporting operation at 150 °C ambient temperature.

2 Features and benefits

2.1 General

- ISO 11898-2:2024 parameter set A-C, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Implements CAN Signal Improvement Capability as defined in ISO 11898-2:2024 parameter Set C to significantly reduce signal ringing effects in a network
- Tighter bit timing symmetry performance versus standard CAN FD transceivers allowing for data rates up to 8 Mbit/s
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- VIO input for interfacing with 3.3 V to 5 V microcontrollers
- Listen-only mode for node diagnosis and failure containment
- Available in SO14 and leadless HVSON14 (3.0 mm x 4.5 mm) packages; HVSON14 with improved Automated Optical Inspection (AOI) capability.
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the battery voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pins, to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby and Sleep modes, with local (WAKE pin), bus (CANH/CANL pins) and host (STB/EN pins) wake-up capability
- Entire node with TJA1463 can be powered down while still supporting local, bus and host wake-up
- CAN wake-up receiver powered by V_{BAT} allowing V_{IO} and V_{CC} to be shut down
- CAN wake-up pattern filter time of 0.5 μs to 1.8 μs, meeting Classical CAN and CAN FD requirements

2.4 Diagnosis & Protection

- Overtemperature diagnosis
- Transmit Data (TXD) dominant time-out and TXD-to-RXD short-circuit handler with diagnosis
- Bus dominant failure diagnosis
- Cold start diagnosis (first battery connection)
- High ESD handling capability on the bus pins
- Bus pins and VBAT protected against transients in automotive environments
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	operating range	4.5	-	28	V
I_{BAT}	battery supply current	Normal or Listen-only mode	-	80	300	µA
		Standby or Sleep mode	-	13	26	µA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin VBAT		4	-	4.5	V
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode, dominant	-	42	70	mA
		Normal mode, recessive	-	7	10	mA
		Listen-only mode	-	5	8	mA
		Standby or Sleep mode	-	-	2	µA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC	$V_{BAT} > 4.5$ V	4	-	4.5	V
$V_{uvhys(VCC)}$	undervoltage hysteresis voltage on pin VCC		50	-	-	mV
V_{IO}	supply voltage on pin VIO		2.95	-	5.5	V
I_{IO}	supply current on pin VIO	Normal mode, dominant; $V_{TXD} = 0$ V	-	90	250	µA
		Normal or Listen-only mode, recessive; $V_{TXD} = V_{IO}$	-	-	3	µA
		Standby or Sleep mode	-	-	2	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	$V_{BAT} > 4.5$ V	2.65	-	2.95	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin VIO		50	-	-	mV
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH and CANL	-6	-	+6	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC 60134	-36	-	+40	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC 60134	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1463AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1463ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

Table 3. TJA1463 feature overview

See Section 18 for a feature overview of the complete TJx14(41/42/43/48)x, TJx14(62/63)x , TJF1441 family.

Device[1]	Modes					Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD	Signal improvement[2]	Wake-up source recognition[3]	Short WUP support [0.5 - 1.8 µs][4]	Single supply pin wake-up[5]	TXD dominant time-out	Local diagnostics via ERR_N pin
TJA1463A	●	●	●	●		●	●	●	●	●	●	●	●	●	●	●

[1] TJA1463 is AEC-Q100 Grade 1.

[2] CAN FD Signal Improvement Capability (SIC) according to ISO 11898-2:2024 parameter set C.

[3] RXD is held LOW after wake-up request, enabling wake-up source recognition.

[4] WUP = wake-up pattern according to Figure 7 in ISO 11898-2:2024.

[5] Only VBAT supply needed for wake-up.

5 Block diagram

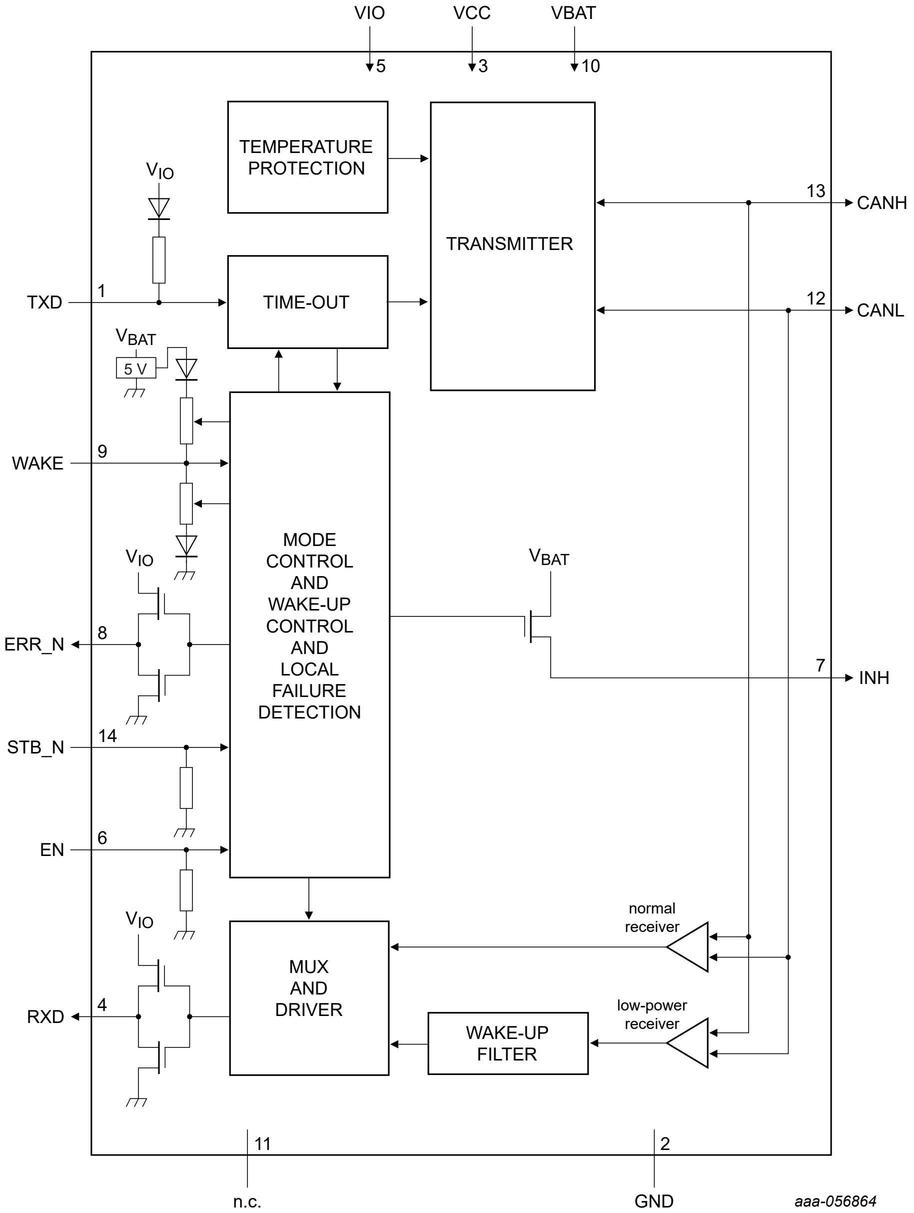
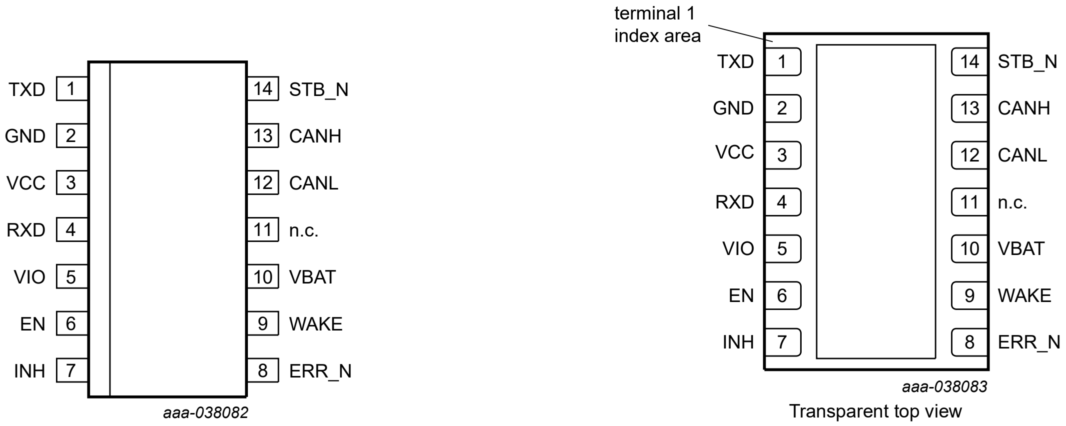


Figure 1. TJA1463 block diagram

6 Pinning information

6.1 Pinning



TJA1463AT: SO14

TJA1463ATK: HVSON14

Figure 2. Pin configuration diagrams

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
GND[2]	2	G	ground
VCC	3	P	5 V supply voltage input
RXD	4	O	receive data output; outputs data read from the bus lines (to the CAN controller)
VIO	5	P	supply voltage input for I/O level adapter
EN	6	I	enable control input
INH	7	AO	inhibit output for switching external voltage regulators
ERR_N	8	O	local failure detection; wake-up source recognition and power-on indication output (active-LOW)
WAKE	9	AI	local wake-up input
VBAT	10	P	battery supply voltage input
n.c.	11	-	not connected
CANL	12	AIO	LOW-level CAN bus line
CANH	13	AIO	HIGH-level CAN bus line
STB_N	14	I	Standby mode control input (active-LOW)

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Operating modes

The TJA1463 contains two independent state machines, a system state machine and a CAN state machine. Two state machines are needed to secure flag handling during undervoltage conditions. These state machines support a number of interdependent operating modes. The system state machine controls the CAN state machine, but both state machines are independently affected by the V_{CC} undervoltage status. For both state machines, undervoltage detection is defined as $V_x < V_{uvd(x)}$ for $t > t_{det(uv)}$ and undervoltage recovery is defined as $V_x > V_{uvd(x)}$ for $t > t_{rec(uv)}$.

7.1.1 System operating modes

The system state machine in the TJA1463 supports five system operating modes. Control pins STB_N and EN are used to select the operating mode. Figure 3 describes how to switch between operating modes. Mode changes are completed after transition time $t_{t(moch)}$. Fail-safe diagnostic information, as described in Section 7.2, is available on pin ERR_N with a delay of $t_{d(moch-ERR\_N)}$ after a mode change.

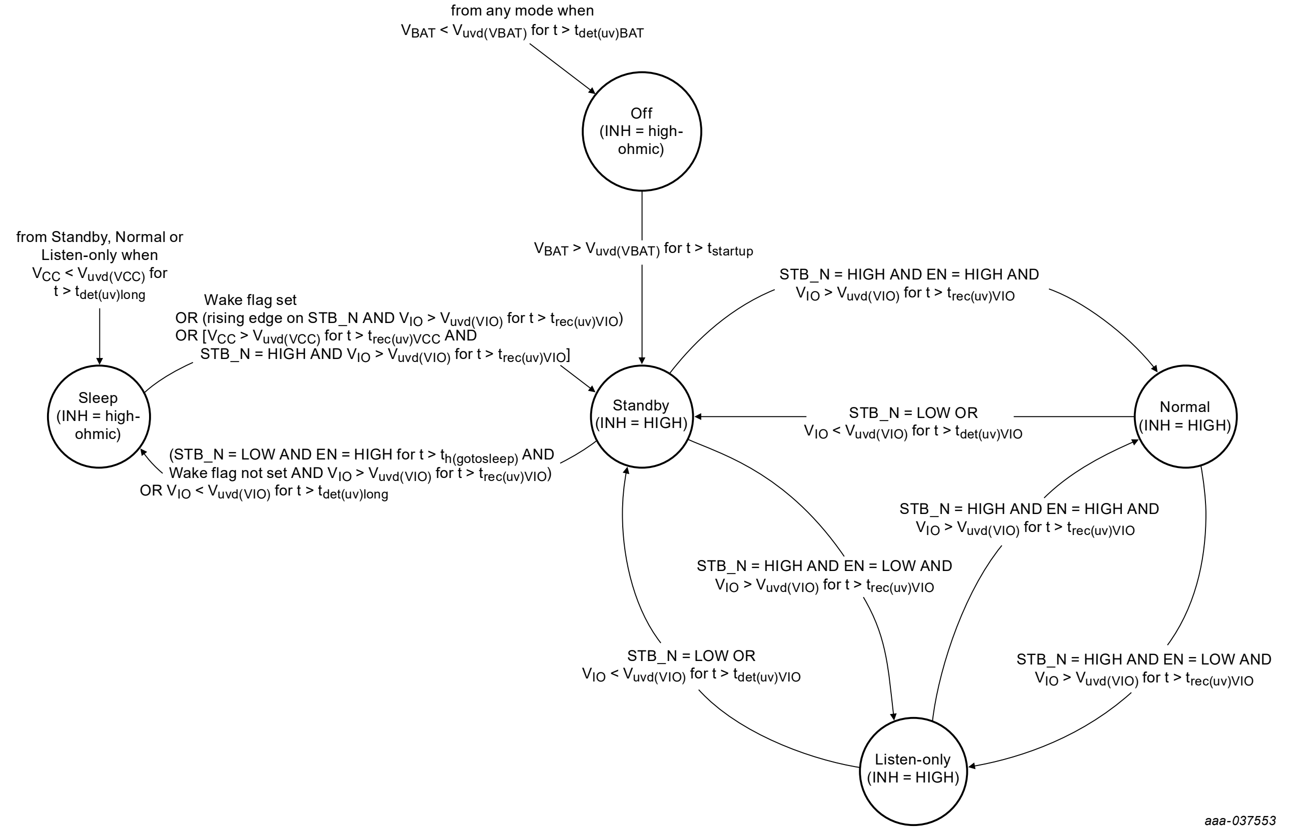


Figure 3. TJA1463 system state diagram

7.1.1.1 Off mode

The TJA1463 switches to Off mode from any mode mode when the battery voltage falls below the undervoltage detection threshold, $V_{uvd(VBAT)}$. The device starts up in Off mode when the battery is connected for the first time (cold start). Pins INH and ERR_N are in a high-ohmic state in Off mode.

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the TJA1463. When V_{BAT} rises above the undervoltage detection threshold, $V_{uvd(VBAT)}$, the TJA1463 starts to boot up, triggering an initialization procedure. It switches to Standby mode after $t_{startup}$, resulting in a HIGH level on pin INH.

When V_{IO} rises above the undervoltage detection threshold, $V_{uvd(VIO)}$, the TJA1463 switches to Normal mode if pins STB_N and EN are HIGH, and to Listen-only mode if STB_N is HIGH and EN is LOW. It will remain in Standby mode if STB_N is LOW.

The TJA1463 will switch to Sleep mode if V_{IO} remains below $V_{uvd(VIO)}$ for $t_{det(uv)long}$ and/or V_{CC} remains below $V_{uvd(VCC)}$ for $t_{det(uv)long}$. A transition from Standby mode to Sleep mode can also be triggered by holding STB_N LOW and EN HIGH for $t_{h(gotosleep)}$ (also known as a 'go-to-sleep' command). This 'go-to-sleep' command is overruled if the Wake flag is set, in which case the device remains in Standby mode.

7.1.1.3 Normal mode

HIGH levels on pin STB_N and pin EN selects Normal mode, provided the battery supply voltage, V_{BAT}, and V_{IO} are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active (see Figure 10).

7.1.1.4 Listen-only mode

A HIGH level on pin STB_N and a LOW level on pin EN selects Listen-only mode, provided V_{BAT} and V_{IO} are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active.

In Listen-only mode the receiver is enabled, but the transmitter is disabled.

7.1.1.5 Sleep mode

Sleep mode is the second-level power-saving mode of the TJA1463. Sleep mode is entered in a number of ways:

- via Standby mode, in response to a 'go-to-sleep' command
- via Standby mode as a result of a V_{IO} undervoltage longer than $t_{det(uv)long}$
- via all other modes, except Off mode, as a result of a V_{CC} undervoltage longer than $t_{det(uv)long}$

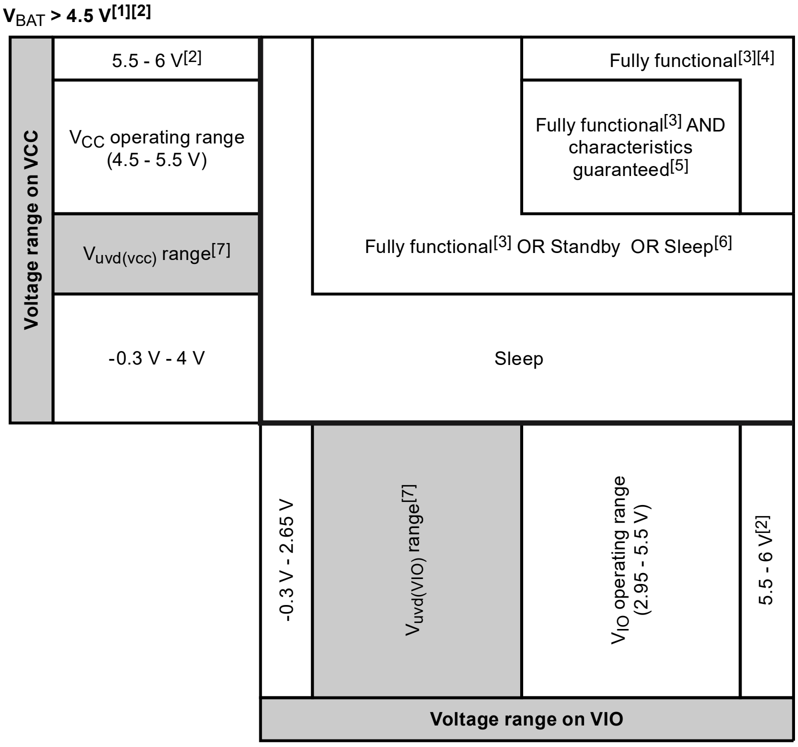
In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set high-ohmic. Voltage regulators controlled by this pin are switched off and the current into pin VBAT is reduced to a minimum.

A number of events will cause the TJA1463 to exit Sleep mode, switching to Standby mode:

- setting the Wake flag
- a rising edge on pin STB_N (if $V_{IO} > V_{uvd(VIO)}$)
- $V_{CC} > V_{uvd(VCC)}$, $V_{IO} > V_{uvd(VIO)}$, STB_N = HIGH and the ‘go-to-sleep’ command has not been activated. After entering Standby mode, the TJA1463 will enter Normal or Listen-Only if STB_N is HIGH.

7.1.1.6 System operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 4.



[1] V_{BAT} operating range is 4.5 V - 28 V and the undervoltage detection threshold range, $V_{uvd(BAT)}$, is 4 V - 4.5 V. For V_{BAT} < 4 V, the device is in Off state. For 4 V ≤ V_{BAT} ≤ 4.5 V the device is either in Off state (if a V_{BAT} undervoltage has been triggered) or in the state as shown in this diagram (if a V_{BAT} undervoltage has not been triggered). For 28 V < V_{BAT} < 40 V this diagram applies, with the single exception that the datasheet characteristics are not guaranteed.

[2] 6 V is the IEC 60134 Absolute Maximum Rating (AMR) for VCC and VIO, 40 V the AMR for VBAT (see Limiting values table). Above the AMR, irreversible changes in characteristics, functionality or performance may occur. Returning from above AMR to the operating range, datasheet characteristics and functionality cannot be guaranteed.

[3] Target transceiver functionality as described in the datasheet is applicable.

[4] Prolonged operation of the device outside the operating range may impact reliability over lifetime. Returning to the operating range, datasheet characteristics are guaranteed provided the AMR has not been exceeded.

[5] Datasheet characteristics are guaranteed within the V_{BAT}, V_{CC} and V_{IO} operating ranges. Exceptions are described in the Static and Dynamic characteristics tables.

[6] For a given value of V_{CC} and V_{IO}, a specific device will be in a single defined state, determined by its undervoltage detection thresholds $V_{uvd(VCC)}$ and $V_{uvd(VIO)}$. The actual thresholds can vary between devices (within the ranges specified in this datasheet). To guarantee the device will be in a specific state, V_{CC} and V_{IO} must be either above the maximum or below the minimum thresholds specified for these undervoltage detection ranges.

[7] The device is fully functional when both V_{CC} and V_{IO} are above the undervoltage threshold. If V_{CC} or V_{IO} is below the undervoltage threshold, the device will be in Standby or Sleep mode.

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Figure 4. TJA1463 supply voltage ranges and gap-free operation

7.1.2 CAN operating modes

The CAN state machine supports six operating modes.

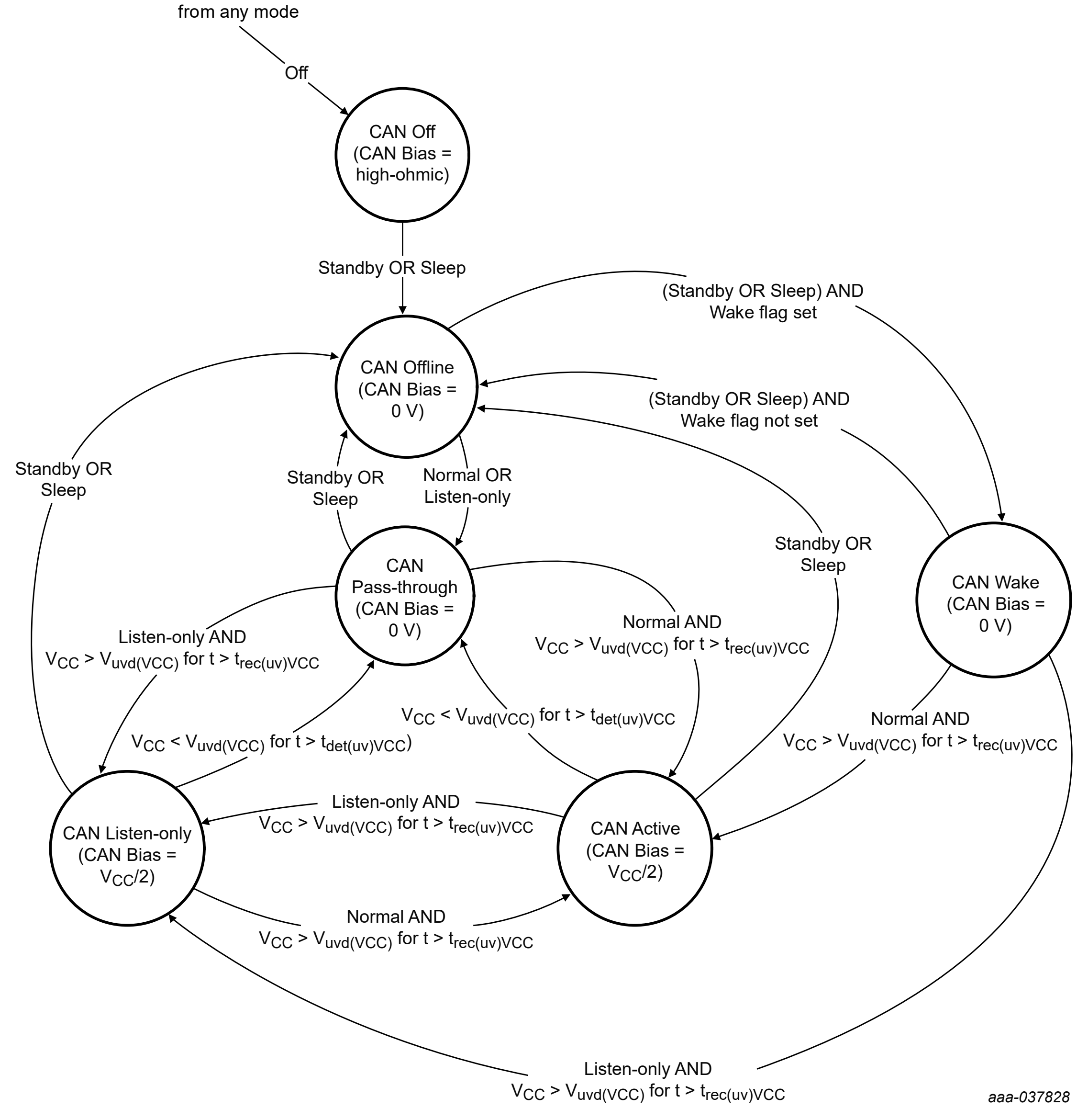


Figure 5. TJA1463 CAN state diagram

7.1.2.1 CAN Off mode

When the TJA1463 system state machine is in Off mode, the CAN state machine will be in CAN Off mode, with the bus pins and pin RXD in a high-ohmic state.

7.1.2.2 CAN Offline mode

When the TJA1463 system state machine is in Sleep or Standby mode and the Wake flag has not been set, the CAN state machine will be in CAN Offline mode. The bus pins are biased to ground.

The transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor the bus for a wake-up pattern. Pin RXD is HIGH.

7.1.2.3 CAN Wake mode

When the TJA1463 system state machine is in Sleep or Standby mode and the wake flag has been set, the CAN state machine will be in CAN Wake mode. Pin RXD will be LOW, reflecting the active wake-up request. The bus pins are biased to ground.

7.1.2.4 CAN Pass-through mode

When the TJA1463 system state machine is in Normal or Listen-only mode and V_{CC} is below the undervoltage detection threshold, $V_{uvd(VCC)}$, the CAN state machine will be in CAN Pass-through mode.

The transceiver cannot transmit data via the bus lines in this mode. The output voltage on the bus pins is biased to ground. Differential data on the bus pins is converted to digital data via the low-power receiver and the results are output on pin RXD.

7.1.2.5 CAN Active mode

When the TJA1463 system state machine is in Normal mode and V_{CC} is above the undervoltage detection threshold, $V_{uvd(VCC)}$, the CAN state machine will be in CAN Active mode. The transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in CAN Active mode before the first transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

7.1.2.6 CAN Listen-only mode

When the TJA1463 system state machine is in Listen-only mode and V_{CC} is above the undervoltage detection threshold, $V_{uvd(VCC)}$, the CAN state machine will be in CAN Listen-only mode. The transmitter is disabled. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. As in CAN Active mode, the bus pins are biased to $V_{CC}/2$.

7.2 Internal flags

The device makes use of four internal flags for fail-safe fallback control and system diagnosis. These flags can be polled by the controller via pin ERR_N while V_{IO} is active. Which flag is available on pin ERR_N at any time depends on the current system operating mode; see Table 5.

Table 5. Accessing internal flags via pin ERR_N

Internal flag	Flag available on pin ERR_N[1]	Flag status: set[2]	Flag status: not set[2]	Flag cleared
Pwon	in Listen-only mode (coming from Standby or Sleep mode)	V_{BAT} has risen above $V_{uvd(VBAT)}$	V_{BAT} has not risen above $V_{uvd(VBAT)}$	on entering Normal mode
Wake	in Standby and Sleep modes (provided V_{IO} and V_{BAT} are present)	remote or local wake-up detected OR Pwon flag has been set	no remote or local wake-up detected	on entering Normal mode or long VIO/ VCC undervoltage
Wake-up source	in Normal mode	local wake-up OR Pwon flag has been set	remote wake-up OR no wake-up	on leaving Normal mode
Local failure	in Listen-only mode (coming from Normal mode)	on occurrence of: - TXD dominant failure OR - TXD-RXD short circuit OR - Bus dominant failure OR - Overtemperature	none of the set conditions have been met	when Pwon flag is set or, provided all local failures have been resolved, when: - device enters Normal mode OR - RXD dominant while TXD recessive OR - bus dominant failure resolved AND no other local failure has set the flag

[1] Pin ERR_N is an active-LOW output; a LOW level indicates a set flag and a HIGH level indicates the flag has not been set.
[2] Status since flag was last cleared.

7.2.1 Pwon flag

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin VBAT recovers after previously dropping below $V_{uvd(VBAT)}$ (usually because the battery was disconnected). The Pwon flag can be used for cold start diagnosis. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. Coming from Sleep or Standby and entering Listen-Only mode, a LOW level on pin ERR_N signals that the Pwon flag has been set. The flag is cleared when the transceiver enters Normal mode.

7.2.2 Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request.

7.2.2.1 Local wake-up (via WAKE pin)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{wake}. The system state machine can set the Wake flag in Standby or Sleep mode. Setting the Wake flag clears the t_{wake} timer. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided V_{IO} and V_{BAT} are present). This flag is also set at power-on and cleared when the transceiver enters Normal mode.

7.2.2.2 Remote wake-up (via the CAN bus)

The TJA1463 wakes up from Sleep to Standby mode when a dedicated wake-up pattern (according to Figure 7 in ISO 11898-2: 2024) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pins RXD and ERR_N remain HIGH until the wake-up event has been triggered and then switch LOW after $t_{startup(RXD)}$/$t_{startup(ERR\_N)}$. Pin INH remains floating until the wake-up event has been triggered and then switches HIGH after $t_{startup(INH)}$.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} undervoltage is detected

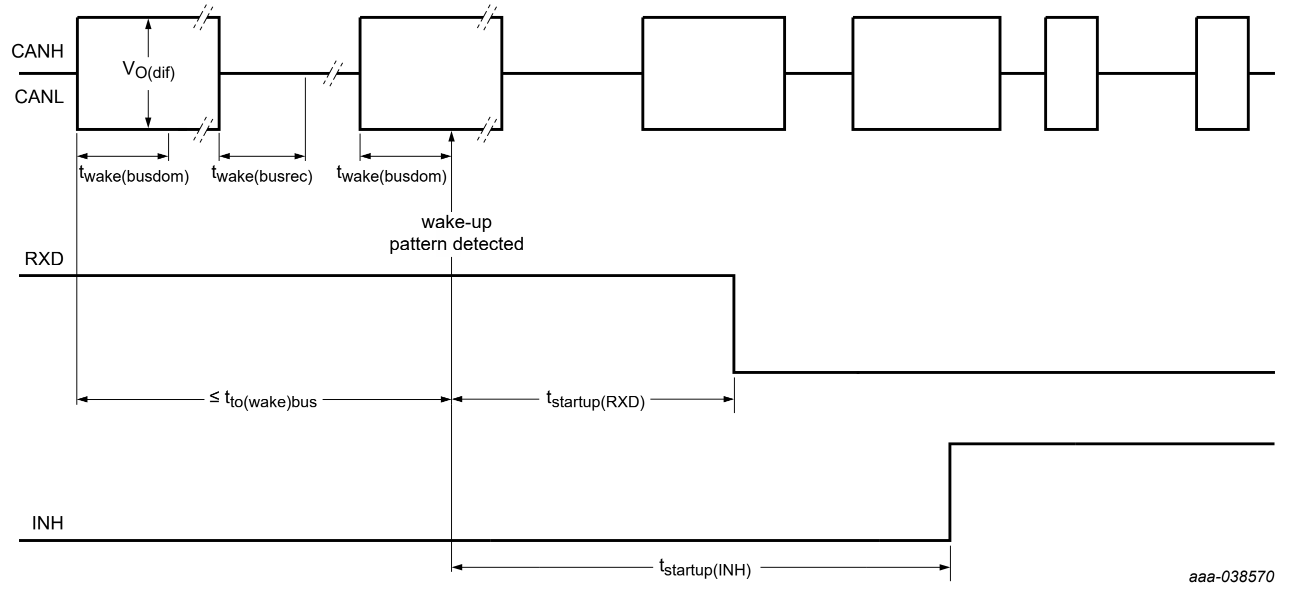


Figure 6. TJA1463 wake-up timing

7.2.3 Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag. It is set after the Wake flag has been set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode (see Table 5). This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

7.2.4 Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four local failure events, any of which will cause the Local failure flag to be set. The four local failure events are:

- TXD dominant failures
- TXD-to-RXD short circuit
- Bus dominant failures
- Overtemperature

The nature and detection of these local failures is described in Section 7.3. The Local failure flag can be polled via the ERR_N pin in Listen-only mode, when coming from Normal mode (see Table 5).

This flag is cleared at power-on when the Pwon flag is set or, provided all local failures have been resolved, when:

- The device enters Normal mode OR
- RXD is dominant while TXD is recessive OR
- Bus dominant failure has been resolved AND no other local failure has set the flag

7.3 Local failure events

The TJA1463 can detect four different local failure conditions, any of which will set the Local failure flag. In most cases, the transmitter is disabled.

7.3.1 TXD dominant failures

A hardware and/or software application failure that caused pin TXD to be held LOW would drive the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out function prevents such a network lock-up. A 'TXD dominant time-out' timer is started when pin TXD goes LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. The transmitter remains disabled until the Local failure flag has been cleared. The TXD dominant time-out timer is reset when pin TXD is set HIGH.

7.3.2 TXD-to-RXD short circuit

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

7.3.3 Bus dominant failures

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not begin to transmit while the bus is dominant, the host controller would not be able to detect this failure condition. However, bus dominant clamping detection will detect the short circuit. The Local failure flag is set if the dominant state on the bus persists for longer than $t_{to(dom)bus}$. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag is reset as soon as the bus returns to recessive state.

7.3.4 Overtemperature

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. The transmitter will remain disabled until the junction temperature drops below $T_{j(sd)rel}$ and the Local failure flag has been cleared.

7.4 I/O levels

Pin VIO should be connected to the same supply voltage used to supply the microcontroller. This adjusts the signal levels on pins TXD, RXD, STB_N, EN and ERR_N to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Spurious signals from the microcontroller on pins STB_N and EN are filtered out with a filter time of $t_{fltr(IO)}$.

7.5 WAKE pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin when V_{WAKE} crosses the wake-up threshold, $V_{th(wake)}$. After the transition, the new HIGH or LOW level should remain stable for at least t_{WAKE}. This allows for maximum flexibility when designing a local wake-up circuit.

A local wake-up is guaranteed in the case of:

- a LOW-to-HIGH transition from $V_{WAKE} < V_{th(wake)min}$ to $V_{WAKE} > V_{th(wake)max}$, followed by $V_{WAKE} > V_{th(wake)max}$ for $t > t_{WAKE(max)}$
- a HIGH-to-LOW transition from $V_{WAKE} > V_{th(wake)max}$ to $V_{WAKE} < V_{th(wake)min}$, followed by $V_{WAKE} < V_{th(wake)min}$ for $t > t_{WAKE(max)}$

A local wake-up is guaranteed not to occur for a transient (L-H-L or H-L-H) of duration $t < t_{(WAKE)min}$, irrespective of the V_{WAKE} voltage level.

To minimize current consumption, the internal bias voltage follows the logic state on the pin after a delay of t_{WAKE}. A HIGH level on pin WAKE is followed by an internal pull-up to 5 V (see Figure 1). A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that do not make use of the local wake-up facility, it is recommended to connect the WAKE pin to pin VBAT or GND for optimal EMI performance.

7.6 Internal biasing of TXD, STB_N and EN input pins

Pin TXD has an internal pull-up to V_{IO} and pins STB_N and EN have internal pull-downs to GND to ensure a safe, defined state in case one, or all, of these pins is left floating. Pull-up/pull-down resistors are present on these pins in all states. Pull-down on pin EN is only active when V_{BAT} is present.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	Voltage on pin x[1]	pins VCC, VIO, TXD, STB_N, EN	-0.3	+6	V
			-	+7[2]	V
		pin VBAT, load dump	-	+40[3]	V
		pin INH	-0.3	V_{BAT}+0.3[4]	V
		pins CANH, CANL, WAKE	-36	+40	V
		pins RXD, ERR_N	-0.3	V_{IO}+0.3[5]	V
$I_{O(INH)}$	output current on pin INH		-2	-	mA
$I_{r(VBAT)}$	reverse current on pin VBAT	assuming the voltage on pin VBAT is below ground level	-10	-	mA
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V
V_{trt}	transient voltage	on pins VBAT, WAKE, CANH, CANL [6]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [7]			
		on pins CANH, CANL	-6	+6	kV
		on pin VBAT with 100 nF capacitor; pin WAKE with 33 kΩ resistor	-8	+8	kV
		SAE J2962-2:2019 (330 pF, 2kΩ) on pins CANH, CANL [8]			
		powered air discharge	-15	+15	kV
		powered contact discharge	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [9]	-4	+4	kV
		on pins CANH, CANL [10]	-8	+8	kV
		Charged Device Model (CDM) [11]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[12]	-40	+150	°C
T_{stg}	storage temperature	[13]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.

[3] For a maximum of 50 hours over the product lifetime.

[4] Absolute maximum of 40 V under the conditions defined in Table note 3 above.

[5] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXD, STB_N and EN.

[6] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637, Part 2.

[7] Verified by an external test house according to IEC TS 62228, Section 4.3.

[8] Verified by an external test house according to ISO 10605.

[9] According to AEC-Q100-002.

[10] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 10). HBM pulse as specified in AEC-Q100-002 used.

[11] According to AEC-Q100-011.

[12] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[13] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 7. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO14	74	K/W
		HVSON14	46	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	HVSON14	13	K/W
$\Psi_{j\text{-}top}$	thermal characterization parameter from junction to top of package	SO14	13	K/W
		HVSON14	7	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 8. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	4	-	4.5	V
V_{uvhys}	undervoltage hysteresis voltage		50	-	-	mV
I_{CC}	supply current	Normal mode				
		dominant; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$	-	42	70	mA
		V_{TXD} = 0 V; -3 V < (V_{CANH} = V_{CANL}) < +40 V; short circuit on bus lines	-	-	125	mA
		Normal mode, recessive; V_{TXD} = V_{IO}	-	7	10	mA
		Listen-only mode	-	5	8	mA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	2	µA
I/O level adapter supply; pin VIO						
V_{IO}	supply voltage		2.95	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	2.65	-	2.95	V
V_{uvhys}	undervoltage hysteresis voltage		50	-	-	mV

Table 8. Static characteristics_...continued_

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IO}	supply current	Normal mode, dominant; V_{TXD} = 0 V	-	90	250	µA
		Normal mode, recessive, V_{TXD} = V_{IO} or Listen-only mode	-	-	3	µA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	2	µA
Supply; pin VBAT						
V_{BAT}	battery supply voltage		4.5	-	28	V
V_{uvd}	undervoltage detection voltage	[2]	4	-	4.5	V
I_{BAT}	battery supply current	Normal or Listen-only mode; pin INH left open	-	80	300	µA
		Normal or Listen-only mode; pin INH left open; T_{vj} ≤ 25 °C; V_{BAT} = 14.5 V	-	80	100	µA
		Standby mode; pin INH left open; V_{WAKE} = V_{BAT} or GND; T_{vj} < 85 °C	-	13	26	µA
		Sleep mode; V_{WAKE} = V_{BAT} or GND; T_{vj} < 85 °C	-	13	26	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[3]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	1	-	10	mA
Standby and enable control inputs; pins STB_N and EN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pd}	pull-down resistance	[4]	20	-	80	kΩ
C_i	input capacitance	[3]	-	-	10	pF
Local failure detection and power-on indication output; pin ERR_N						
I_{OH}	HIGH-level output current	V_{ERR_N} = V_{IO} - 0.4 V	-50	-	-4	µA
I_{OL}	LOW-level output current	V_{ERR_N} = 0.4 V	0.1	-	2	mA
Local wake-up input; pin WAKE						
R_{pu}	pull-up resistance	V_{WAKE} > $V_{th(wake)(max)}$ for t > $t_{wake(max)}$	100	-	400	kΩ

Table 8. Static characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pd}	pull-down resistance	$V_{WAKE} < V_{th(wake)(min)}$ for $t > t_{wake(max)}$	100	-	400	kΩ
$V_{th(wake)}$	wake-up threshold voltage	Sleep or Standby mode	1.8	-	2.6	V
V_{hys}	hysteresis voltage		90	-	-	mV
Inhibit output; pin INH						
ΔV_H	HIGH-level voltage drop	$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -1 mA	0	-	1	V
		$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -2 mA	0	-	2	V
I_L	leakage current	Sleep mode; Off mode	-2	-	+2	μA
$I_{O(sc)}$	short-circuit output current	V_{INH} = 0 V	-15	-	-	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		pin CANH; R_L = 50 Ω to 65 Ω	2.89	3.5	4.26	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.77	1.5	2.13	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [3] [5]	0.9V_{CC}	-	1.1V_{CC}	V
$V_{cm(step)}$	common mode voltage step	[3] [5] [6]	-150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[3] [5] [6]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V [5]				
		R_L = 50 Ω to 65 Ω	1.5	-	2.75	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω [3]	1.5	-	5	V
		recessive; no load				
		Normal or Listen-only mode; $V_{TXD} = V_{IO}$	-50	-	+50	mV
		Standby or Sleep mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal or Listen-only mode; $V_{TXD} = V_{IO}$; no load	2	2.5	3	V
		Standby or Sleep mode; no load	-0.1	0	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		Normal or Listen-only mode	0.5	-	0.9	V
		Standby or Sleep mode	0.4	-	1.1	V

Table 8. Static characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{rec(RX)}$	receiver recessive voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		Normal or Listen-only mode	-8	-	+0.5	V
		Standby or Sleep mode	-8	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		Normal or Listen-only mode	0.9	-	9	V
		Standby or Sleep mode	1.1	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V; Normal or Listen-only mode	100	-	-	mV
$I_{O(sc)}$	short-circuit output current	-15 V ≤ V_{CANH} ≤ +40 V; -15 V ≤ V_{CANL} ≤ +40 V	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	-27 V ≤ V_{CANH} ≤ +32 V; -27 V ≤ V_{CANL} ≤ +32 V; Normal or Listen-only mode; V_{TXD} = V_{IO} for t > $t_{d(TXD-buspasrec)start}$ [7]	-3	-	+3	mA
I_L	leakage current	V_{CC} = V_{IO} = V_{BAT} = 0 V or pins shorted to GND via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	-10	-	+10	μA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V; passive recessive[8]	25	40	50	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V; passive recessive [8]	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V; passive recessive [8]	50	80	100	kΩ
$C_{i(cm)}$	common-mode input capacitance	[3]	-	-	30	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	15	pF
Signal Improvement function on CANH or CANL; +4.75 V ≤ V_{CC} ≤ +5.25 V; see Figure 9						
$R_{i(dom)}$	dominant phase input resistance	bus dominant; V_{CC} - 1.6 V ≤ V_{CANH} ≤ V_{CC} - 1.2 V; +1.2 V ≤ V_{CANL} ≤ +1.6 V; $R_{i(dif)dom}$ = $R_{i(dom)CANH}$ + $R_{i(dom)CANL}$	-	-	30	Ω
$R_{i(dif)dom}$	dominant phase differential input resistance		-	-	60	Ω
$R_{i(actrec)}$	active recessive phase input resistance[9]	bus dominant-to-recessive transition [10] +1.5 V ≤ V_{CANH} ≤ V_{CC} - 1.5 V; +1.5 V ≤ V_{CANL} ≤ V_{CC} - 1.5 V; $R_{i(dif)actrec}$ = $R_{i(actrec)CANH}$ + $R_{i(actrec)CANL}$	37.5	-	62.5	Ω
$R_{i(dif)actrec}$	active recessive phase differential input resistance[9]		75	-	125	Ω

Table 8. Static characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[3]	180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature	[3]	175	-	195	°C

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.

[3] Not tested in production; guaranteed by design.

[4] Pull-down on EN pin is only active when V_{BAT} is present.

[5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in Figure 12.

[6] See Figure 7.

[7] This parameter is defined in ISO 11898-2:2024 parameter set C and is specified in the Dynamic Characteristics table (see Table 9 and Figure 9).

[8] Passive recessive in accordance with ISO 11898-2. Input impedance is passive once the signal improvement phase has come to an end (active recessive end).

[9] Active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD. The maximum value specified is lower than proscribed in ISO11898-2:2024 parameter set C (a lower value is preferred).

[10] Both conditions and the maximum specified values are tighter, thus better than prescribed in ISO11898-2:2024 parameter set C.

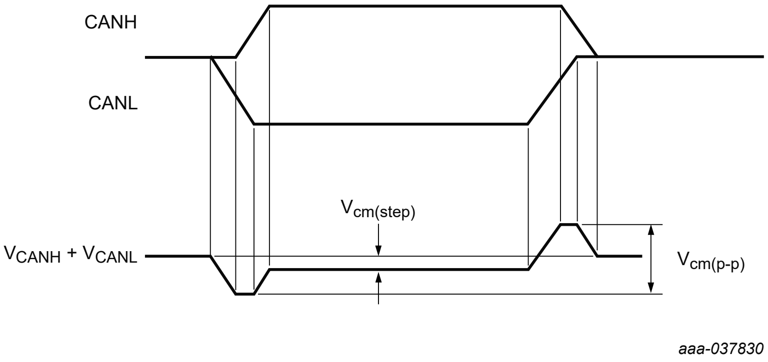


Figure 7. CAN bus common-mode voltage according to SAE 1939-14

11 Dynamic characteristics

Table 9. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics according to ISO 11898-2:2024; see Figure 8 and Figure 11						
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	255	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	255	ns
CAN timing characteristics according to ISO 11898-2:2024; V_{CC} = 4.75 V to 5.25 V; see Figure 8, Figure 9 and Figure 11						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	80	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	80	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or Listen-Only mode	-	-	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or Listen-Only mode	-	-	110	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start	Normal mode [2] [3]	415	-	530	ns
$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start	Normal mode [2]	70	-	120	ns
$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end	Normal mode [2]	355	-	480	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)} \geq$ 125 ns, up to 8 Mbit/s)[4]; V_{CC} = 4.75 V to 5.25 V; see Figure 8 and Figure 11						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-10	-	+10	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-20	-	+15	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-30	-	+20	ns
CAN FD timing characteristics ($t_{bit(TXD)} \geq$ 200 ns, up to 5 Mbit/s) [5]; see Figure 8 and Figure 11						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-30	-	+30	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-45	-	+15	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-50	-	+40	ns
Dominant time-out times						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [2] [6]	0.8	-	9	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)}$ > 0.9 V; Normal or Listen-Only mode [2] [6]	0.8	-	9	ms
Bus wake-up times; pins CANH and CANL; see Figure 6						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby or Sleep mode [2] [7]	0.5	-	1.8	μs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby or Sleep mode [2] [7]	0.5	-	1.8	μs

Table 9. Dynamic characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V; V_{BAT} = 4.5 V to 28 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(wake)bus}$	bus wake-up time-out time	Standby or Sleep mode [2] [6]	0.8	-	9	ms
Mode transitions; see Section 7.1 and Figure 6						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	μs
$t_{startup}$	start-up time	[2]	-	-	1.5	ms
$t_{startup(RXD)}$	RXD start-up time	after local or remote wake-up detected [2] [8]	4	-	20	μs
$t_{startup(INH)}$	INH start-up time	after local or remote wake-up detected; transition from Sleep to Standby [2] [9]	4	-	50	μs
$t_{startup(ERR\_N)}$	ERR_N start-up time	after local or remote wake-up detected [2]	4	-	20	μs
$t_{h(gotosleep)}$	go-to-sleep hold time	STB_N = LOW and EN = HIGH hold time for entering Sleep mode [2] [10]	24	-	50	μs
$t_{d(moch-ERR\_N)}$	delay time from mode change to ERR_N	to ERR_N stable in response to a mode transition [2]	-	-	20	μs
Local wake-up input; pin WAKE						
t_{WAKE}	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode [11]	20	-	50	μs
IO filter; pins STB_N, EN						
$t_{fltr(IO)}$	I/O filter time	[12]	1	-	5	μs
Undervoltage detection; see Section 7.1.1 and Figure 5						
$t_{det(uv)}$	undervoltage detection time	on pin VBAT [2]	-	-	30	μs
		on pin VCC [2]	-	-	30	μs
		on pin VIO [2]	-	-	30	μs
$t_{det(uv)long}$	long undervoltage detection time	on pins VCC and/or VIO [2] [13]	100	-	150	ms
$t_{rec(uv)}$	undervoltage recovery time	on pin VCC [2]	-	-	50	μs
		on pin VIO [2]	-	-	50	μs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Not tested in production; guaranteed by design.

[3] If TXD goes LOW before the recessive transition has been completed, the bus switches to dominant.

[4] Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s) and B ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbit/s).

[5] For reasons related to CAN FD bit timing symmetry, these values are centered around the nominal bit length. Details can be found in document AH2002 'TJx144x/TJx146x Application Hints', available on request from NXP Semiconductors

[6] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[7] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[8] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 6.

[9] INH switches HIGH between the min and max values after a wake-up had been detected. INH is guaranteed to be floating below the min value and guaranteed to be HIGH above the max value; see Figure 6.

[10] The device is guaranteed to switch to Sleep mode when STB_N = LOW and EN = HIGH for longer than max value, and guaranteed not to switch to Sleep mode when less than the min value.

[11] The device is guaranteed to wake up above 50 μs and guaranteed not to wake up below 20 μs.

[12] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

[13] An undervoltage longer than the max value is guaranteed to force a transition to Sleep mode; an undervoltage shorter than the min value is guaranteed not to force a transition to Sleep mode.

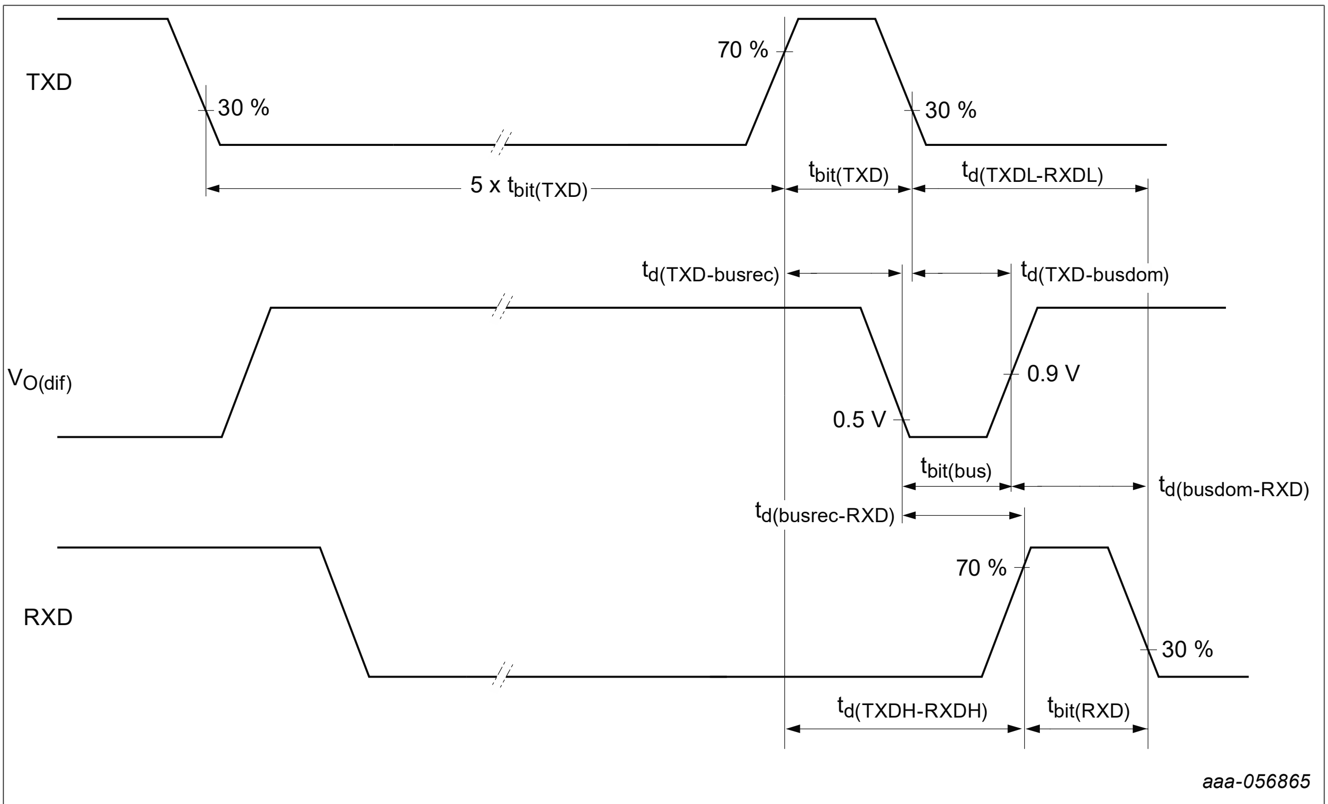
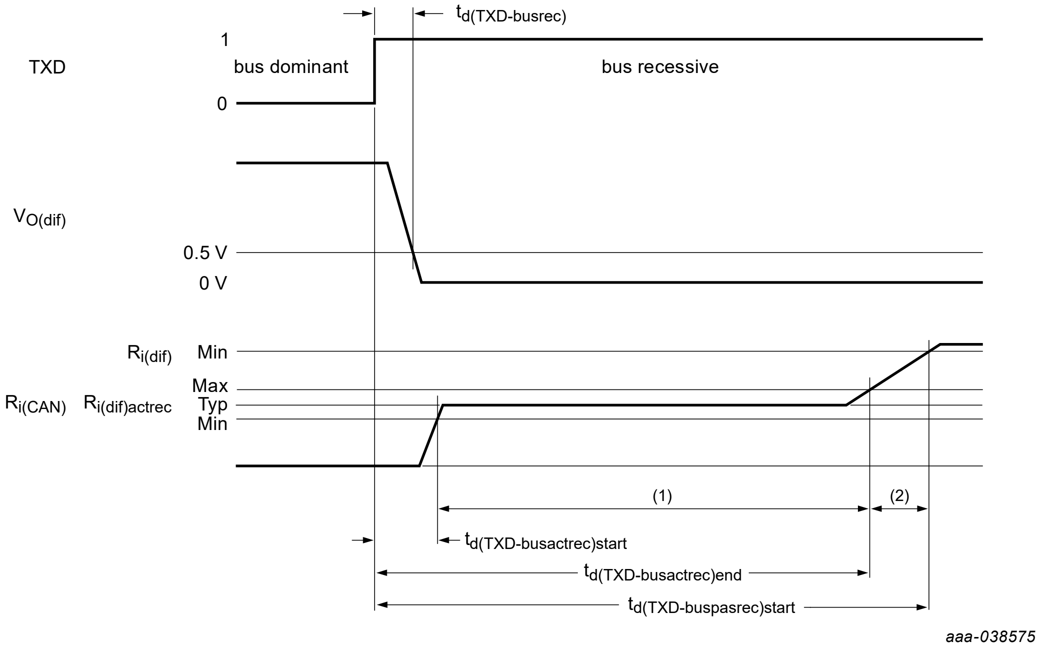


Figure 8. CAN transceiver timing diagram according to ISO 11898-2:2024

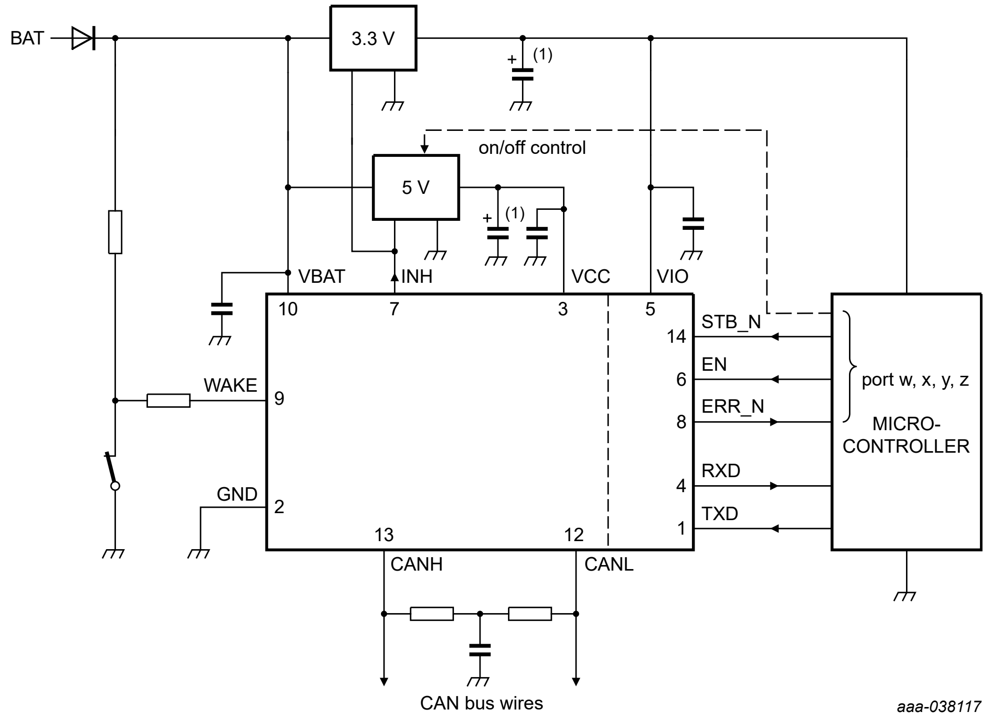


(1) Active recessive phase (2) Release phase.

Figure 9. Transmitter impedance and timing diagram for dominant-to-passive recessive transition according to ISO11898-2:2024 parameter set C

12 Application information

12.1 Application diagram



(1) Optional, depends on regulator.

Figure 10. Typical TJA1463 application with a 3.3 V microcontroller

12.2 Application hints

Further information on the application of the TJA1463 can be found in NXP application hints AH2002 *'TJx144x/ TJx146x Application Hints'*, available on request from NXP Semiconductors.

13 Test information

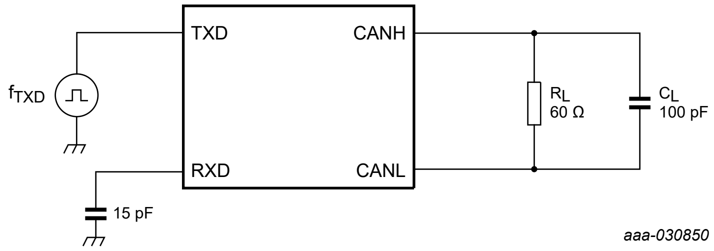


Figure 11. CAN transceiver timing test circuit

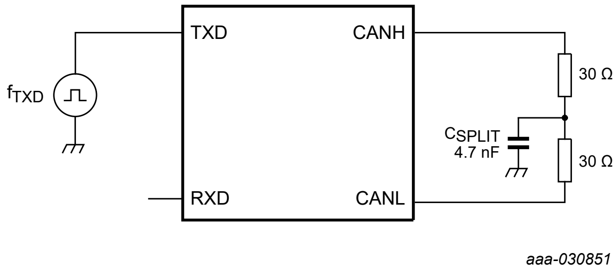


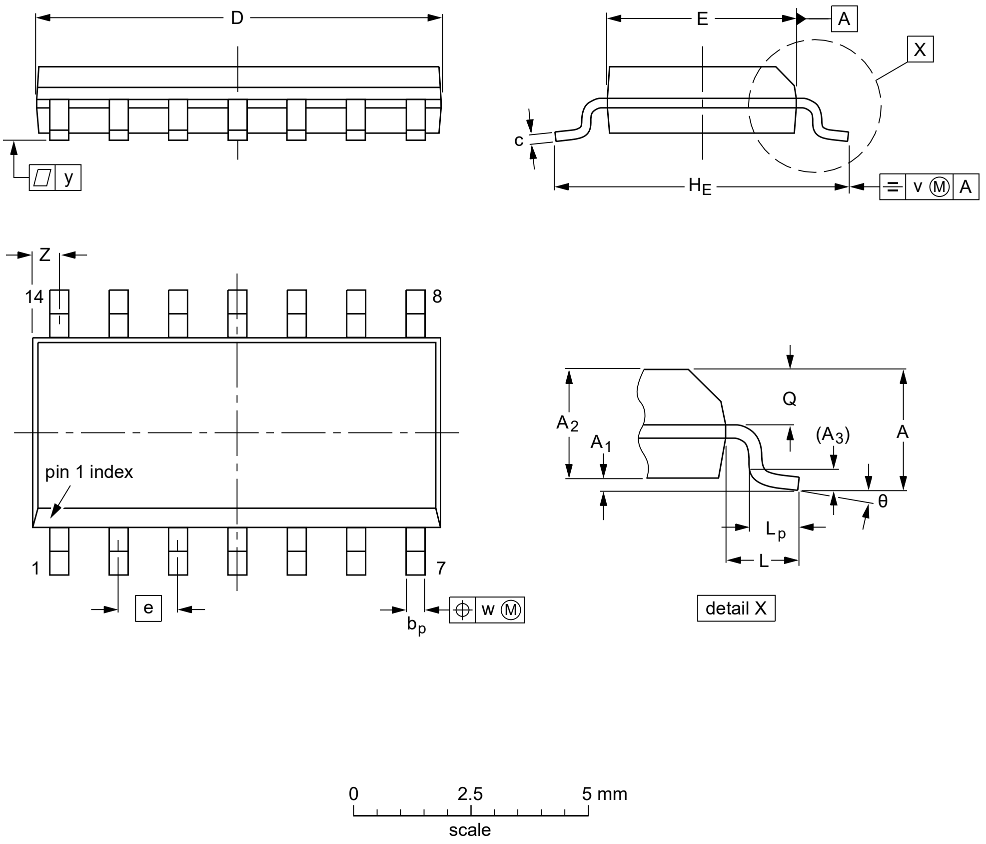
Figure 12. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

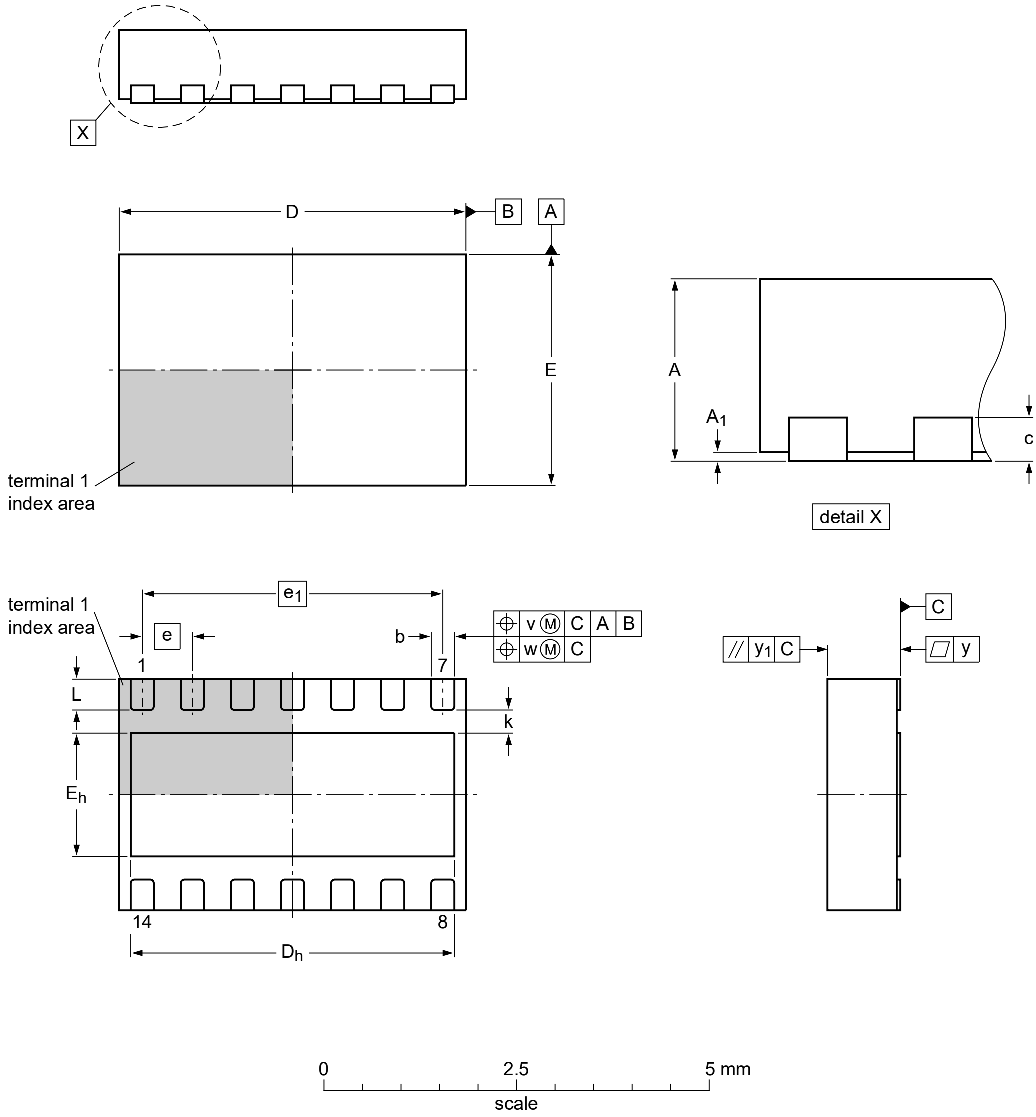
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 13. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 14. Package outline SOT1086-2 (HVSON14)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

Table 10. SnPb eutectic process (from J-STD-020D)

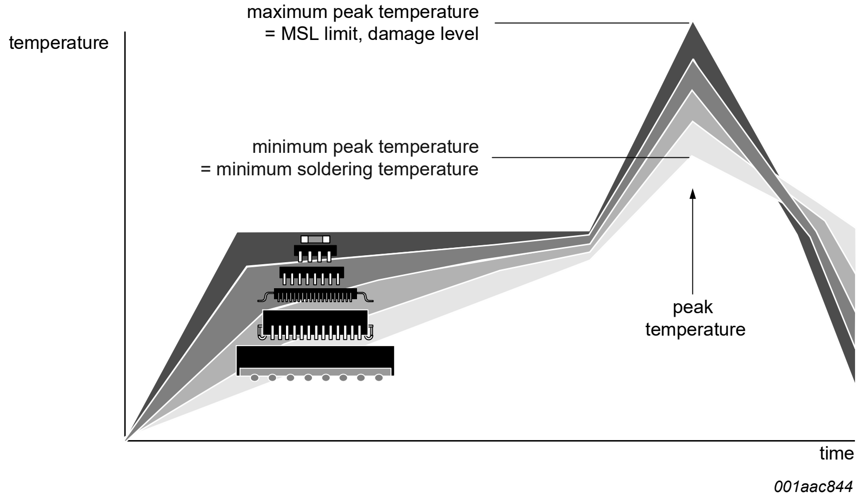
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.



MSL: Moisture Sensitivity Level

Figure 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17 Appendix: ISO 11898-2:2024 parameter cross-reference lists

Table 12. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	$R_{DIFF\_pas\_rec}$	$R_{i(dif)}$	differential input resistance
Single-ended internal resistance	$R_{SE\_pas\_rec\_H}$ $R_{SE\_pas\_rec\_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry			
Driver symmetry	V_{sym_vcc}	V_{TXsym}	transmitter voltage symmetry
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time

Table 12. ISO 11898-2:2024 to NXP data sheet parameter conversion[1] *...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA implementation loop delay requirements for parameter sets A, B and C			
Loop delay for parameter sets A and B	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
Loop delay for parameter set C		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD\_BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS\_RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominent to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter sets A, B and C			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C			
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF\_act\_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Internal single-ended resistance	$R_{SE\_act\_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Start time of active signal improvement phase	$t_{act\_rec\_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act\_rec\_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas\_rec\_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start
PMA voltage wake-up control timing			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH)}$	INH start-up time
		$t_{startup(ERR\_N)}$	ERR_N start-up time
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits before a SOF is accepted
BitFilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter\_option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter\_option2}$		
HS-PMA bus biasing control timing			
Time-out for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	bus bias reaction time

[1] A number of proprietary NXP parameters are equivalent to parameters defined in ISO 11898-2:2024, but use different symbols. This conversion table allows ISO parameters to be cross-referenced with their NXP counterparts. The NXP parameters are defined in the Static and Dynamic characteristics tables. The conversion table provides a comprehensive listing - individual devices may not include all parameters.

18 Appendix: TJx14(41/42/43/48)x, TJx14(62/63)x , TJF1441 family overview

Table 13. Feature overview of the complete TJx14(41/42/43/48)x, TJx14(62/63)x , TJF1441 family

Device[1]	Modes				Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD[2]	Signal improvement[3]	Wake-up source recognition[4]	Short WUP support [0.5 - 1.8 µs][5]	Single supply pin wake-up[6]	TXD dominant time-out	Local diagnostics via ERR_N pin
TJx1441A	●			●	●	●		●						●	
TJx1441B	●			●	●			●						●	
TJx1441D	●			●	●			●						●	
TJF1441A	●			●	●	●		●						[7]	
TJx1442A	●	●			●	●		●				●	●	●	
TJx1442B	●	●			●			●				●		●	
TJx1443A	●	●	●	●	●	●	●	●			●	●	●	●	●
TJx1448A	●	●			●	●		●				●	●	●	
TJx1448B	●	●			●			●				●		●	
TJx1448C	●	●			●	●		●			●	●	●	●	
TJx1462A	●	●			●	●		●	●	●		●	●	●	
TJx1462B	●	●			●			●	●	●		●		●	
TJx1463A	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

[1] TJx: TJA14xxx is AEC-Q100 Grade 1; TJR14xxx is AEC-Q100 Grade 0; TJF1441A is non-automotive grade.
[2] Only guaranteed for TJA1462x and TJA1463x, AEC-Q100 Grade 1.
[3] CAN FD signal improvement capability (SIC) according to ISO11898-2:2024 parameter set C.
[4] RXD is held LOW after wake-up request, enabling wake-up source recognition.
[5] WUP = wake-up pattern according to Figure 7 in ISO 11898-2:2024.
[6] Only VIO supply needed for wake-up in TJA1442A, TJA1448A, TJA1448C, TJA1462A; only VBAT supply needed for wake-up in TJA1443A, TJA1463A.
[7] Not having TXD dominant time-out allows for very low data rates in non-automotive grade applications.

19 Revision history

Table 14. Revision history

Document ID	Release date	Description
TJA1463 v.3.0	12 February 2025	• ISO 11898-2:2016 upgraded to ISO 11898-2:2024 throughout • Replaced CiA 601-4:2019 with ISO 11898-2:2024 parameter set C throughout • Section 2.1: 3rd list item revised (on bit timing symmetry) • Table 3: table title and table notes 2 and 4 amended • Section 7.1.1.5: text of last list item amended (STB_N = HIGH added) • Section 7.2.2.1: text changed ('timer' changed to 't_{wake} timer') • Section 7.2.2.2: text of 1st and 4th paragraphs amended ($t_{startup(ERR\_N)}$ added in 4th paragraph) • Section 7.5: text revised • Table 6: – parameter $I_{r(VBAT)}$ added; V_x: pin VBAT min value removed – SAE J2962-2:2019 V_{ESD} entries added • Table 8: – measurement conditions amended: I_{CC}, I_{BAT}, $I_{O(sc)rec}$, I_L, R_i, ΔR_i, $R_{i(dif)}$ – values changed: $V_{rec(RX)}$ – parameters deleted: $R_{i(extdom)}$, $R_{i(dif)extdom}$ – table notes 7 and 8 (now 9) revised – table notes 8 and 10 added • Table 9: – formatting of CAN (FD) timing characteristics revised (including table notes) – parameters added: $t_{d(TXD-buspasrec)start}$, $t_{startup(ERR\_N)}$ – parameter value changed: $t_{d(TXD-busactrec)end}$ (min) – parameters deleted: $t_{d(TXD-busrec)end}$, $t_{d(TXD-busdom)end}$, $t_{d(extbusdom)end}$ • Original Figs. 7 and 8 combined in new single Figure 8 • Redundant Fig. 11 removed • Figure 9 revised (absolute values deleted) • Original Section 17 deleted • Section 18: section title, table title and table notes 2, 3 and 5 amended • Section 17: cross-reference tables updated • Legal information: *HTML publications* disclaimer added
TJA1463 v.2.0	15 October 2021	-
TJA1463 v.1.0	12 August 2020	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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