TJA1465

CAN SIC transceiver with partial networking

Rev. 1.0 — 16 October 2024 Product data sheet

1 General description

The TJA1465 is a high-speed CAN transceiver that provides an interface between a controller area network (CAN) or flexible data rate CAN (CAN FD) protocol controller and the physical two-wire CAN bus. TJA1465 transceivers implement the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5, making them fully interoperable with high-speed classical CAN and CAN FD transceivers. The TJA1465 was developed in compliance with ISO 26262, achieving ASIL B.

The TJA1465 features very low power consumption in Standby and Sleep modes. It supports CAN partial networking by means of selective wake-up functionality as specified in ISO 11898-2:2024, making the TJA1465 the ideal choice for CAN system implementations where only nodes that are needed are to be activated. Nodes that are not needed for the function being performed can be powered down to minimize system power consumption, even when CAN bus traffic is running.

The TJA1465 includes an SPI for configuration, mode control and diagnostics. The TJA1465B additionally features three general-purpose I/O pins (GPIO) and a CAN transmitter enable/disable input.

The TJA1465 can be configured to ignore CAN FD and CAN XL frames while waiting for a valid wake-up frame. This additional feature of partial networking, called CAN FD/XL passive, is the perfect fit for networks that support a mix of classical CAN, CAN FD and CAN XL communication.

In Normal mode, the TJA1465 supports external CAN protocol controllers that communicate according to classical CAN, CAN FD, or CAN XL in SIC mode without switching to FAST mode (according to ISO 11898-2:2024 Annex A).

The TJA1465 features CAN signal improvement capability (SIC), as defined in ISO 11898-2:2024. SIC significantly reduces signal ringing on a network, allowing reliable 2 Mbit/s and 5 Mbit/s CAN FD communication in larger and more complex topologies. Tight bit timing symmetry enables CAN FD communication up to 8 Mbit/s.

2 Features and benefits

2.1 General

- ISO 11898-2:2024 parameter sets A-C, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- ISO 26262, ASIL B compliant
- Partial networking capability through selective wake-up functionality
- Configurable general-purpose I/O (GPIO) pins (TJA1465B)
- Second RXD and/or TXD pins (RXD2/TXD2), configurable via GPIO (TJA1465B)
- Direct transmitter on/off control input (TXEN_N) (TJA1465B)
- CAN signal improvement capability as defined in ISO 11898-2:2024 parameter set C to significantly reduce signal ringing effects on a network

- Autonomous bus biasing
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- VIO input for interfacing with 1.8 V, 3.3 V to 5 V microcontrollers
- ListenOnly mode for node diagnosis and failure containment
- TJA1465A available in an SO14 package and leadless HVSON14 package with automatic optical inspection (AOI) capabilities
- TJA1465B available in a DHVQFN18 package with automatic optical inspection (AOI) capabilities
- Dark green product (halogen free and restriction of hazardous substances (RoHS) compliant)
- Selectable interrupts on RXD; option to signal only wake-up and power-on related interrupts or all interrupts
- 4-byte general-purpose memory
- SPI system reset
- End-of-line microcontroller flashing support through CAN pins
- Selectable WAKE pin filter time

2.2 Predictable and fail-safe behavior

- Undervoltage detection on all supply pins with defined behavior below the undervoltage thresholds
- Functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Transceiver disengages from the bus (high-ohmic) when the battery voltage drops below the Off mode threshold
- Internal biasing of TXD to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby and Sleep modes, with local and remote wake-up capability
- Local wake-up via the WAKE pin
- Remote wake-up via a wake-up pattern (WUP) or wake-up frame (WUF)
- Configurable CAN wake-up pattern (dom-rec-dom or dom-rec-dom-rec) according to ISO 11898-2:2024.
- Selective wake-up according to ISO 11898-2:2024
- Entire node containing the TJA1465 can be powered down via INH while still supporting local and remote wake-up
- Only V_{BAT} is needed to support local and remote wake-up
- Support for pretended networking through low-power ListenOnly mode

2.4 Diagnosis and Protection

- Overtemperature diagnosis and protection
- Transmit data (TXD) dominant time-out diagnosis and protection
- Bus dominant failure diagnosis
- Cold start diagnosis (first battery connection)
- High ESD handling capability on the bus pins
- Bus pins and VBAT protected against automotive transients

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage		4.75	-	40	V
I_{BAT}	battery supply current	Normal mode or (ListenOnly mode; VBATVCC = 1 or LPL = 0); $V_{BAT} \leq 28$ V	-	-	400	µA
		ListenOnly mode; VBATVCC = 0 and LPL = 1; $V_{BAT} \leq 28$ V	-	-	525	µA
		Sleep or Standby mode; CAN Offline Bias mode; partial networking enabled; $T_{vj} < 85$ °C; VBATVCC = 0	-	-	450	µA
		Sleep or Standby mode; CAN Offline mode; $T_{vj} < 85$ °C	-	12	20	µA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin VBAT		4.25	-	4.75	V
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode; transmitter dominant	-	42	60	mA
		Normal or (ListenOnly mode and LPL = 0); transmitter recessive	-	7	10	mA
		ListenOnly mode; LPL = 1; VBATVCC = 1; $T_{vj} < 150$ °C	-	90	165	µA
		ListenOnly mode; LPL = 1; VBATVCC = 0; $T_{vj} < 150$ °C	-	-	40	µA
		Sleep or Standby mode; $T_{vj} < 85$ °C	-	-	3	µA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4	-	4.5	V
V_{IO}	supply voltage		1.71	-	5.5	V
I_{IO}	supply current	Normal or ListenOnly mode (excluding pull-up currents on V_{IO}-related pins)	-	-	5	µA
		Standby or Sleep mode; $T_{vj} < 85$ °C	-	-	2	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO		1.5	-	1.71	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH, CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value	-36	-	+40	V
V_{CANL}	voltage on pin CANL	limiting value	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

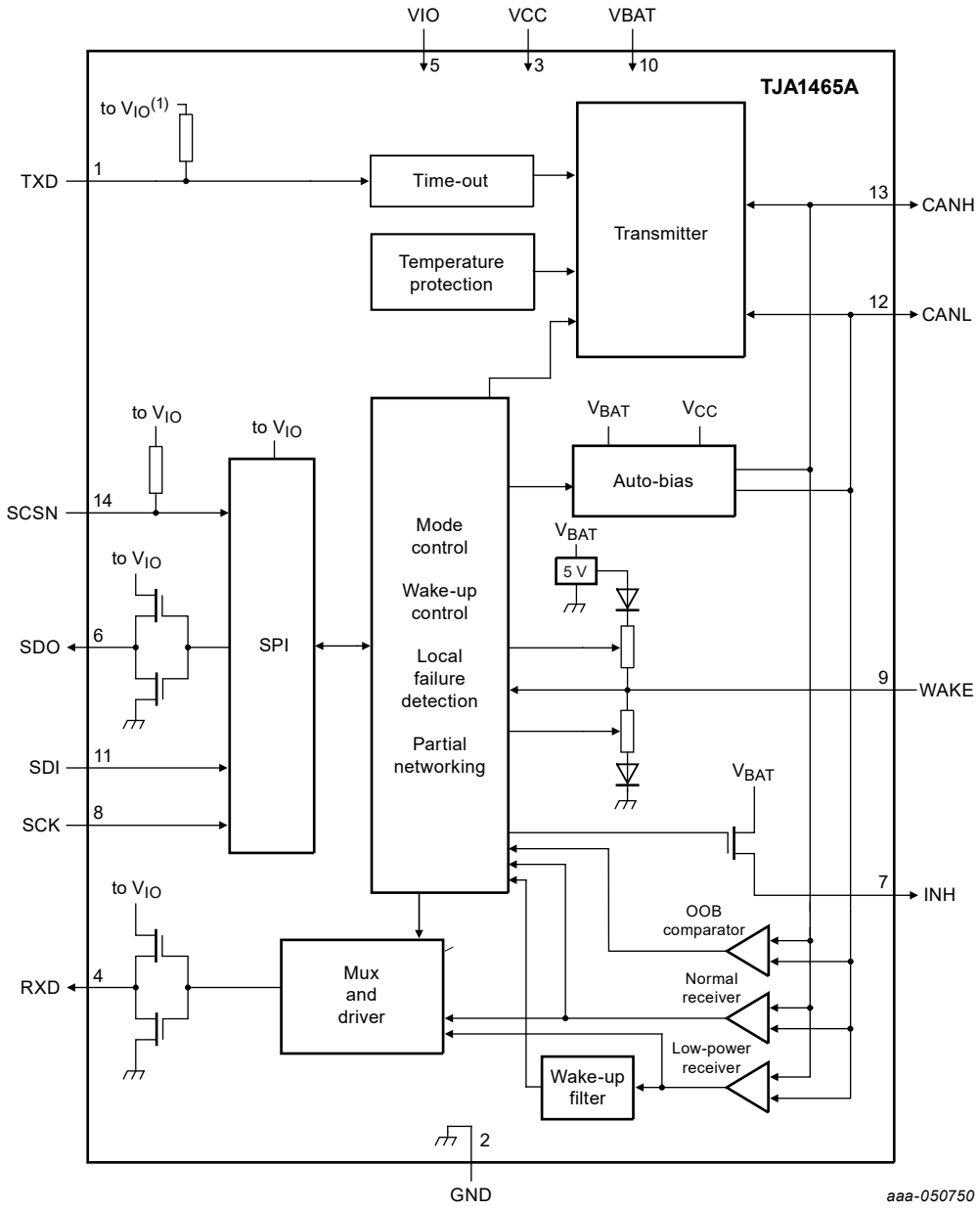
Type number	Package		
	Name	Description	Version
TJA1465AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1465ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
TJA1465BHG	DHVQFN18	plastic thermal enhanced very thin small outline package; no leads; 18 terminals; body 3 × 4.5 × 0.85 mm	SOT2163-1

Table 3. Feature overview of the TJA1465 family

See Section 18 for a feature overview of the complete TJA1445x/TJA1446x/TJA1465x/TJA1466x family.

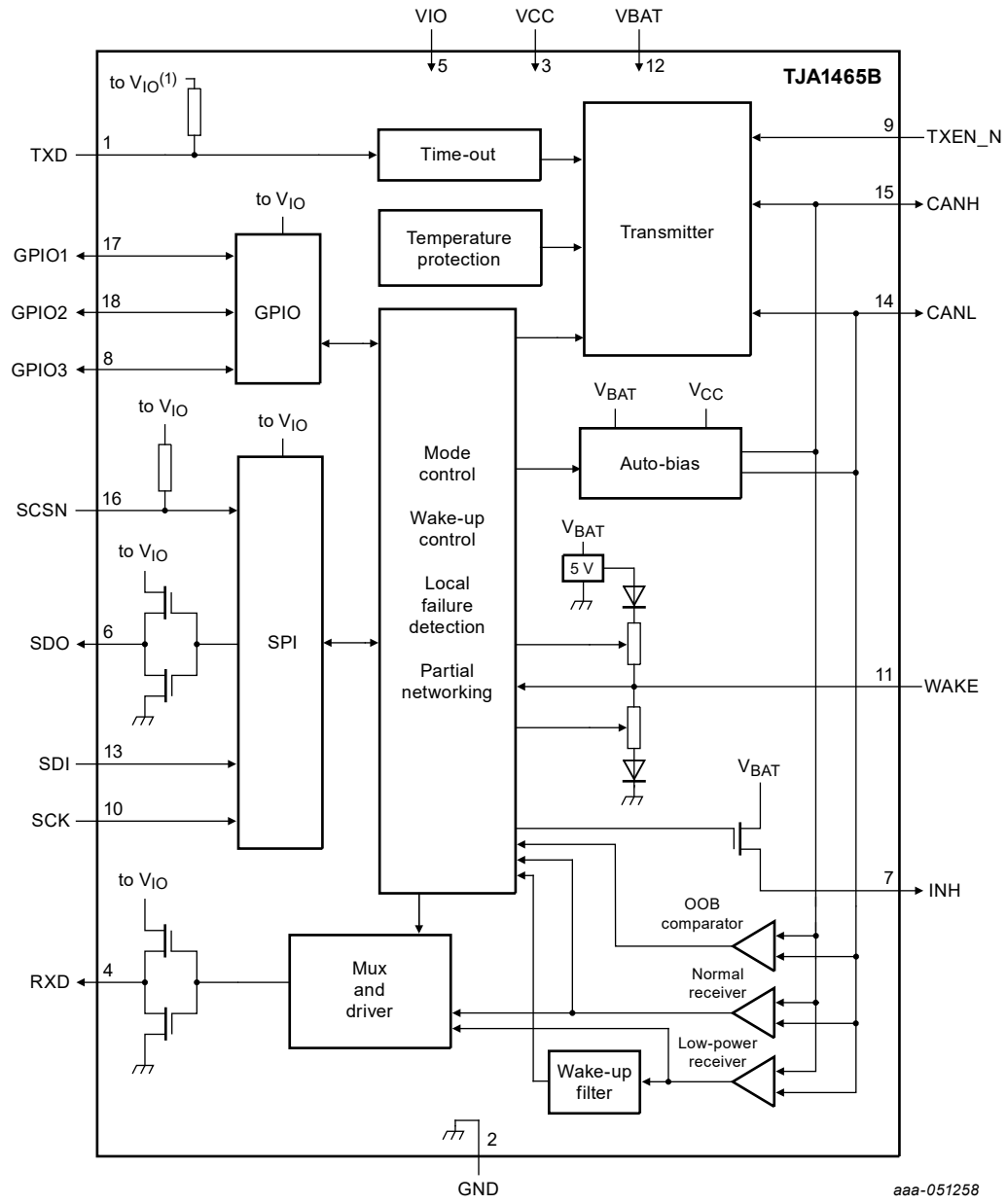
Device	Partial Networking			V_{IO} supply			Data rate		Special features							
	Selective wake-up	CAN FD passive	CAN XL passive	1.8 V V_{IO}	3.3 V V_{IO}	5.0 V V_{IO}	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN SIC	ISO 26262 ASIL B compliance	GPIO pins	TXEN_N pin	RST_N pin	FSO/LIMP pin	V_{IO} undervoltage monitoring	V_{IO} overvoltage monitoring	Q&A watchdog
TJA1465A	●	●	●	●	●	●	●	●	●					●		
TJA1465B	●	●	●	●	●	●	●	●	●	3	●			●		

5 Block diagram



(1) See Table 9.

Figure 1. Block diagram: TJA1465A



(1) See Table 9.

Figure 2. Block diagram: TJA1465B

6 Pinning information

6.1 Pinning

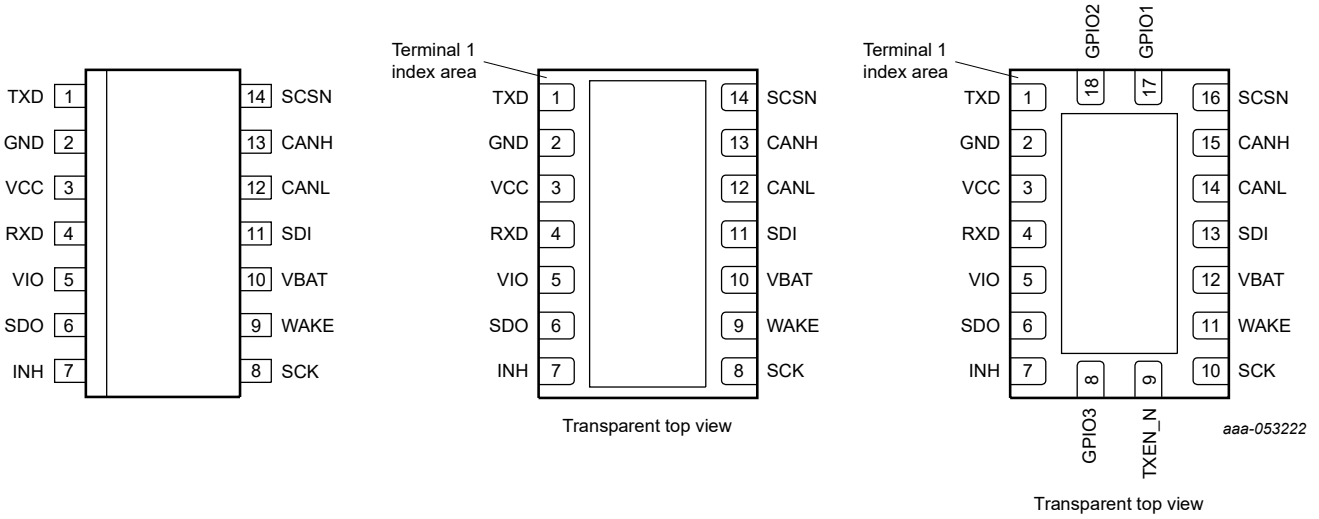


Figure 3. Pin configuration diagrams

6.2 Pin description

Table 4. Pin description: TJA1465A

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND[2]	2	G	ground
VCC	3	P	supply voltage for CAN transmitter
RXD	4	O	receive data output
VIO	5	P	supply voltage for I/O level adapter
SDO	6	O	SPI data output
INH	7	AO	inhibit output for switching external voltage supplies or indicating wake-up from Sleep mode (active-HIGH)
SCK	8	I	SPI clock input
WAKE	9	AI	local wake-up input
VBAT	10	P	battery supply voltage
SDI	11	I	SPI data input
CANL	12	AIO	LOW-level CAN bus line
CANH	13	AIO	HIGH-level CAN bus line
SCSN	14	I	SPI chip select input (active-LOW)

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

Table 5. Pin description: TJA1465B

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND[2]	2	G	ground
VCC	3	P	supply voltage for CAN transmitter
RXD	4	O	receive data output
VIO	5	P	supply voltage for I/O level adapter
SDO	6	O	SPI data output
INH	7	AO	inhibit output for switching external voltage supplies or indicating wake-up from Sleep mode (active-HIGH)
GPIO3	8	I/O	general purpose input/output 3
TXEN_N	9	I/O	CAN transmitter enable/disable input (active-LOW)
SCK	10	I	SPI clock input
WAKE	11	AI	local wake-up input
VBAT	12	P	battery supply voltage
SDI	13	I	SPI data input
CANL	14	AIO	LOW-level CAN bus line
CANH	15	AIO	HIGH-level CAN bus line
SCSN	16	I	SPI chip select input (active-LOW)
GPIO1	17	I/O	general purpose input/output 1
GPIO2	18	I/O	general purpose input/output 2

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] DHVQFN18 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Supply

Table 6. Supply description

Supply pin	Supply	Description
VBAT	V_{BAT}	Main supply for the device, needed for all internal processes; supplies the CAN receivers
VCC	V_{CC}	Supply for the CAN transmitter and for bus biasing
VIO	V_{IO}	Supply and reference level for the digital interface pins TXD and RXD, the SPI interface, TXEN_N and the GPIO pins

7.2 System operating modes

Table 7 contains a summary of the system finite state machine (FSM_MAIN) operating modes. A mode transition diagram is shown in Figure 4. Mode changes are completed after transition time $t_{t(moch)}$. Abbreviations used in the mode transition diagram are defined in Table 8.

Table 7. FSM_MAIN operating modes

Operating mode	Description
Off	Device is deactivated
Boot	Device loads the configuration and registers are reset to default values
Check_SNM	Device checks the CAN bus status
Standby	Device is in the first-level low-power mode with INH active
Sleep	Device is in the second-level low-power mode with INH inactive
ListenOnly	Device is able to receive CAN data from the bus
Normal	Device is able to transmit and receive CAN bus traffic

Table 8. State diagram legend

Category	Abbreviation	Definition
VBAT pin status	BAT_UV	$V_{BAT} < V_{uvd(VBAT)}$ for $t > t_{det(uv)VBAT}$
	BAT_OK	$V_{BAT} > V_{uvd(VBAT)}$ for $t > t_{rec(uv)VBAT}$
Memory check during boot phase	BOOT_OK	passed internal memory consistency check (takes up to $t_{startup}$)
	BOOT_FAIL	failed internal memory consistency check
Start-to-Normal mode check	SNM	CAN bus must remain dominant for $t > t_{t(snm)}$ in Check_SNM mode
	NO_SNM	CAN bus detected recessive in CHECK_SNM mode or valid SPI message detected since Boot mode
Wake-up request status	WAKEUP	valid local or remote wake-up trigger received
	NO_WAKEUP	no valid local or remote wake-up trigger received
Wake-up source selection	WAKESOURCE_SELECTED	local (WAKE) and/or remote wake-up source selected
Temperature status	NO_OVERTEMP	$T_j < T_{j(sd)rel}$
	OVERTEMP	$T_j > T_{j(sd)}$
VIO pin status	VIO_UV_LONG	$V_{IO} < V_{uvd(VIO)}$ for $t > t_{det(uv)long}$
	VIO_OK	$V_{IO} > V_{uvd(VIO)}$ for $t > t_{rec(uv)}$
MCU reaction timeout	MCU_REAC_EXP	no valid SPI activity for $t > t_{to(MCU)}$ with a power-on or wake-up interrupt pending
Mode select	MC_NORMAL	Normal mode (MC = 1111)
	MC_STANDBY	Standby mode (MC = 0110)
	SPI_WRITE_SLEEP (see Section 7.10.1)	Sleep mode command (SPI write MC = 0001)
	MC_LISTENONLY	ListenOnly mode (MC = 1000)
SPI system reset	SPI_RESET	SPI forces system reset (see Section 7.10.2)

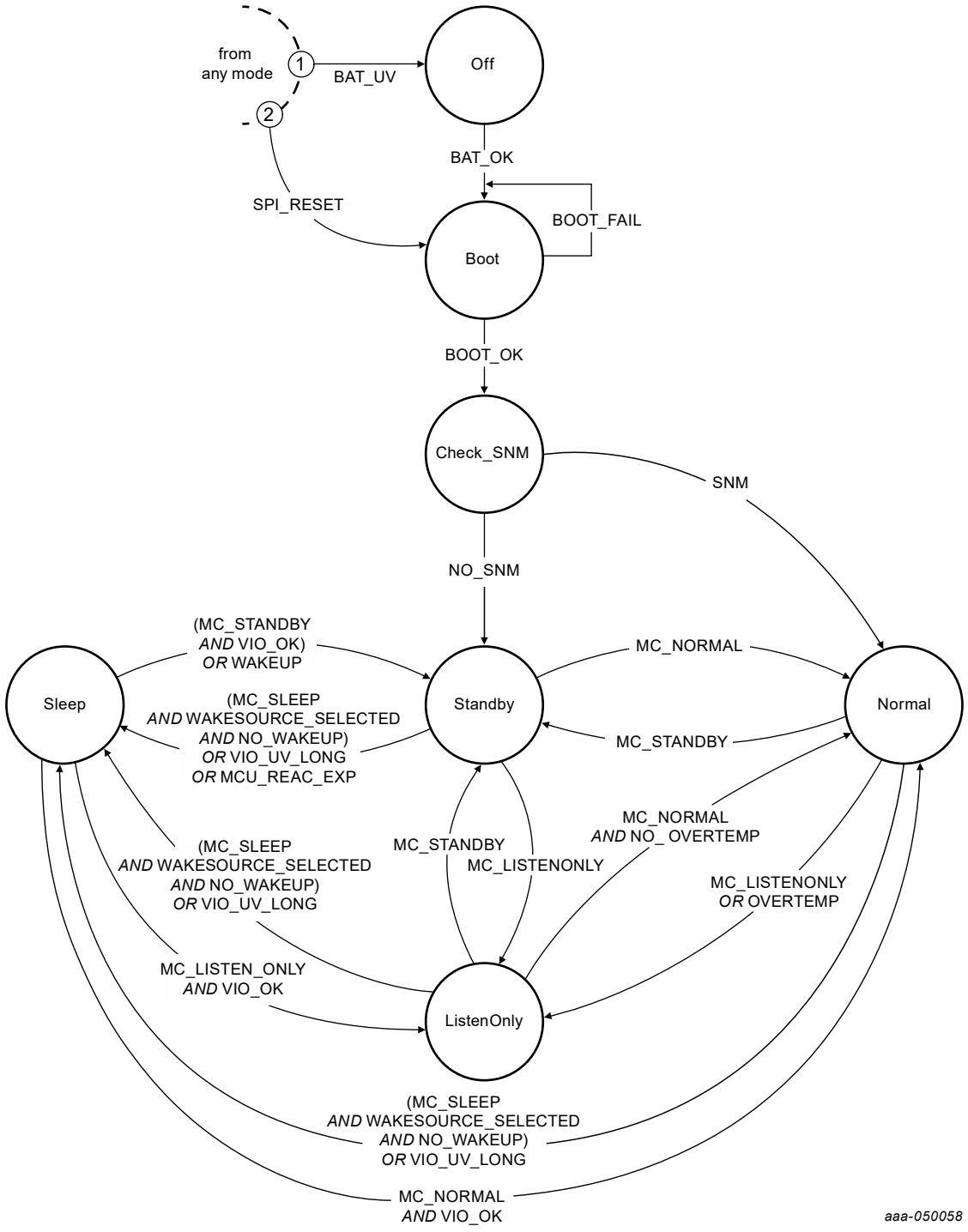


Figure 4. System state diagram (FSM_MAIN)

Transitions that take priority over all others are indicated with priority 1-2 (encircled number at state exit). All other transitions are mutually exclusive.

The device can enter Normal mode directly (SNM) via a boot sequence after power on or a system reset. To pass the SNM check, the CAN bus must be in dominant state before the main state machine enters

Check_SNM mode and must remain dominant for at least t > $t_{t(snm)}$. When Normal mode was entered directly after booting, bit SNMS in the system status register is set to 1.

7.2.1 Pin and functional block states per operating mode

Table 9. Pin state per System operating mode

All supplies within operating range with no error condition present.

Pin	Off/Boot/Check_SNM	Sleep	Standby	ListenOnly	Normal
TXD	high-Z	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH [1]
RXD	high-Z	HIGH or LOW when interrupt pending[2]	HIGH or LOW when interrupt pending[2]	CAN bus status	CAN bus status
SDO	high-Z	high-Z when SCSN HIGH	high-Z when SCSN HIGH	high-Z when SCSN HIGH	high-Z when SCSN HIGH
INH	high-Z	high-Z	HIGH[3]	HIGH[3]	HIGH [3]
SCK	high-Z	repeater	repeater	repeater	repeater
SDI	high-Z	repeater	repeater	repeater	repeater
SCSN	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH [1]	pulled HIGH[1]	pulled HIGH[1]
TJA1465B only					
GPIO1	high-Z	GPIO	GPIO	GPIO	GPIO
GPIO2	high-Z	GPIO	GPIO	GPIO	GPIO
GPIO3	high-Z	GPIO	GPIO	GPIO	GPIO
TXEN_N	LOW	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH [1]

[1] HIGH = driven to V_{IO} level, as defined in Table 49.
[2] Interrupt pending: at least one bit set in one or more interrupt status registers (see Section 7.10.10).
[3] HIGH = driven to V_{BAT} level, as defined in Table 49.

Table 10. Functional state per System operating mode

All supplies within operating range with no error condition present.

Function	SPI configuration	Off/Boot/Check_SNM	Sleep	Standby	ListenOnly	Normal
SPI		off	on	on	on	on
CAN		high-Z	GND or 2.5 V bias (autobias)	GND or 2.5 V bias (autobias)	$V_{CC}/2$[1] bias and receiver active	$V_{CC}/2$ bias and receiver active
Local wake-up		off	on	on	on	on
CAN wake-up	PNCOK = 0	off	on	on	off	off
	PNCOK = 1	off	off	off	off	off
Partial networking	PNCOK = 0	off	off	off	off	off
	PNCOK = 1	off	on	on	on	on
Overtemp		off	off	off	off[2]	on

[1] 2.5 V when LPL = 1.
[2] Overtemperature detection remains active after a transition from Normal mode to ListenOnly mode due to an overtemperature condition.

7.2.2 Local wake-up via the WAKE pin

The device monitors the WAKE pin and can be configured to respond on a rising and/or falling edge:

- A WPR interrupt is generated on a rising edge if WPRE = 1 (see Table 37)
- A WPF interrupt is generated on a falling edge if WPFE = 1 (see Table 37)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{wake}. t_{wake} is configured via bit WFC in Table 36. The WAKE pin status can be read via bit WPS in the System status register (Table 18). The GPIO pins on the TJA1465B can also be configured as V_{IO} level wake pins (see Section 7.8).

7.3 CAN operating modes

Table 11 contains a summary of the CAN finite state machine (FSM_CAN) operating modes. A mode transition diagram is shown in Figure 5. Abbreviations used in the mode transition diagram are defined in Table 12.

Table 11. CAN operating modes

Operating mode	Description
CAN Off	The CAN transceiver is off.
CAN Offline	The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) on the bus.
CAN OfflineBias	The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) or wake-up frame (WUF) on the bus.
CAN ListenOnly	Only the CAN receiver is active and able to capture a wake-up frame (WUF); the RXD pin reflects the CAN bus status.
CAN Active	The CAN transceiver is active and able to capture a wake-up frame (WUF).

Table 12. State diagram legend

Category	Abbreviation	Definition
CAN bus events	BUSSILENCE	CAN bus idle for $t > t_{to(silence)}$
	WUP	valid CAN wake-up pattern detected
VCC pin status	VCC_OK	$V_{CC} > V_{uvd(VCC)}$ for $t > t_{rec(uv)}$
	VCC_UV	$V_{CC} < V_{uvd(VCC)}$ for $t > t_{det(uv)}$

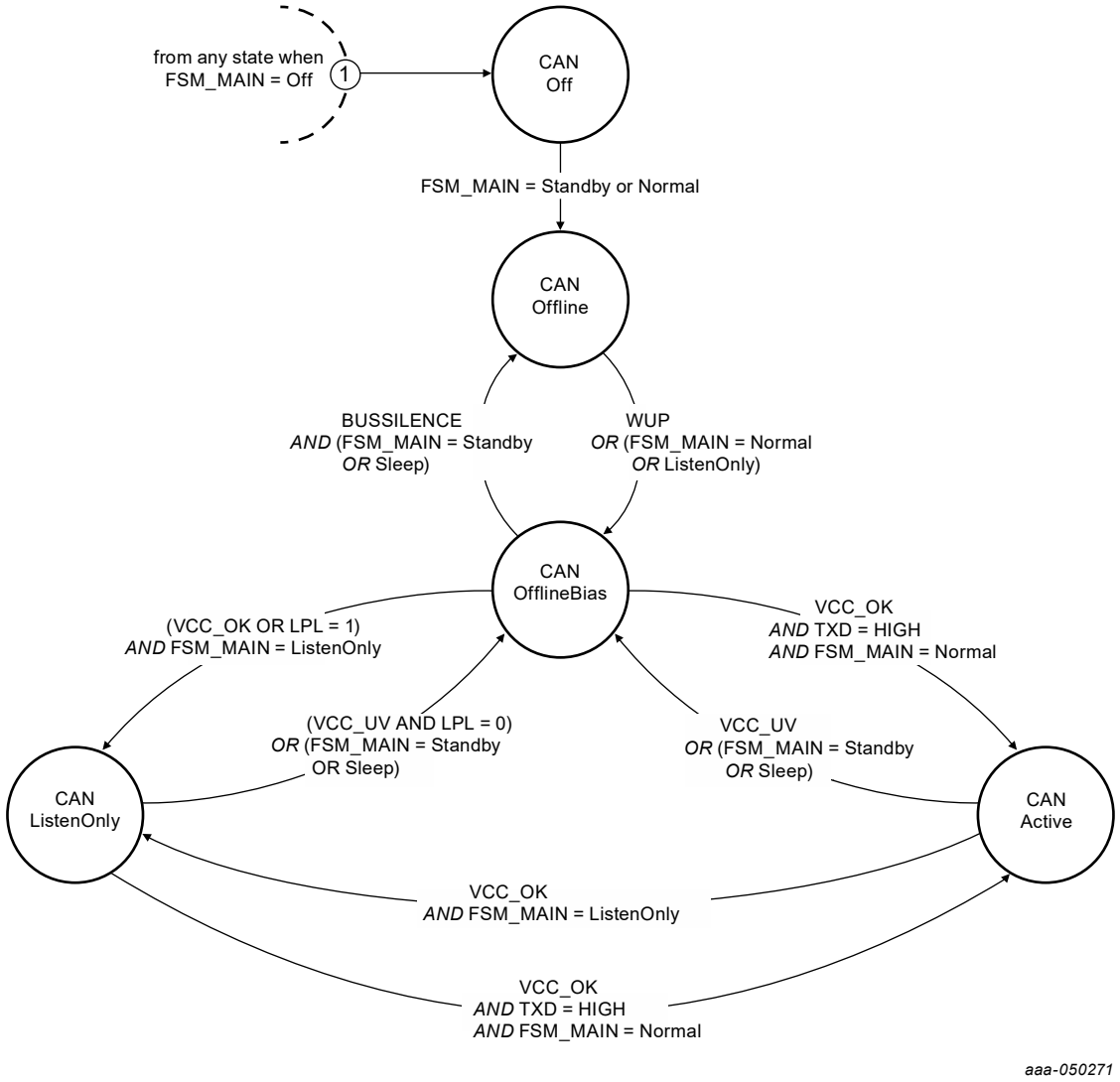


Figure 5. CAN state diagram (FSM_CAN)

State transitions are mutually exclusive. FSM_MAIN = Off condition overrides any transition triggered at the same time, indicated by '1' (priority 1) in Figure 5.

Low-power ListenOnly mode (LPL = 1; see Figure 5 and Table 20) is intended for Pretended Networking use cases and provides CAN listen-only behavior without a V_{CC} supply. In this mode, the CAN transmitter is switched off to minimize quiescent current and CAN bus biasing is derived from V_{BAT} (see Table 13). The receiver operates normally.

7.3.1 Functional block state per CAN operating mode

Table 13. Functional block state per CAN operating mode

Block	SPI configuration	CAN Off	CAN Offline	CAN Offline Bias	CAN Listen Only	CAN Active
CAN transmitter	LPL = 0	off	off	off	recessive	active [1]
	LPL = 1	off	off	off	off	active [1]
CAN receiver		off	off	off	active	active

Table 13. Functional block state per CAN operating mode*...continued*

Block	SPI configuration	CAN Off	CAN Offline	CAN Offline Bias	CAN Listen Only	CAN Active
CAN bias	VBATVCC = 1	high-Z	GND	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
	LPL = 0 and VBATVCC = 0	high-Z	GND	2.5 V derived from V_{BAT}	$V_{CC}/2$	$V_{CC}/2$
	LPL = 1 and VBATVCC = 0	high-Z	GND	2.5 V derived from V_{BAT}	2.5 V derived from V_{BAT}	$V_{CC}/2$

[1] If TXEN_N is HIGH in TJA1465B, status will be recessive

7.3.2 CAN wake-up

The TJA1465 supports remote wake-up via a CAN wake-up pattern (WUP) or selective wake-up via a CAN wake-up frame (WUF).

7.3.2.1 CAN wake-up pattern (WUP)

The CAN wake-up pattern (WUP) is used for two purposes:

- To activate CAN biasing in CAN Offline mode (transition from CAN offline to CAN OfflineBias)
- To trigger a CAN wake-up event

The following conditions must be met to trigger a wake-up event via a CAN WUP:

- The CAN transceiver is in CAN Offline or CAN OfflineBias mode
- CAN wake-up enabled (CWE = 1)
- CAN wake-up frame detection (WUF) deactivated (CPNC = 0 or PNCOK = 0)

The TJA1465 supports both the standard (ISO 11898-2:2024, section 5.5.4) and the extended (ISO 11898-2:2024, section A.4.1) wake-up patterns (see Figure 6 and Figure 7). The WUP is selected via bit CWC in the CAN configuration register (Table 20).

The wake-up pattern consists of:

ISO 11898-2:2024, section 5.5.4, standard WUP

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

ISO 11898-2:2024, section A.4.1, WUP extension

- standard WUP followed by a recessive phase of at least $t_{wake(busrec)}$

Dominant or recessive bits between the phases shorter than $t_{wake(busdom)}$ or $t_{wake(busrec)}$, respectively, are ignored.

The complete wake-up pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6 and Figure 7). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event.

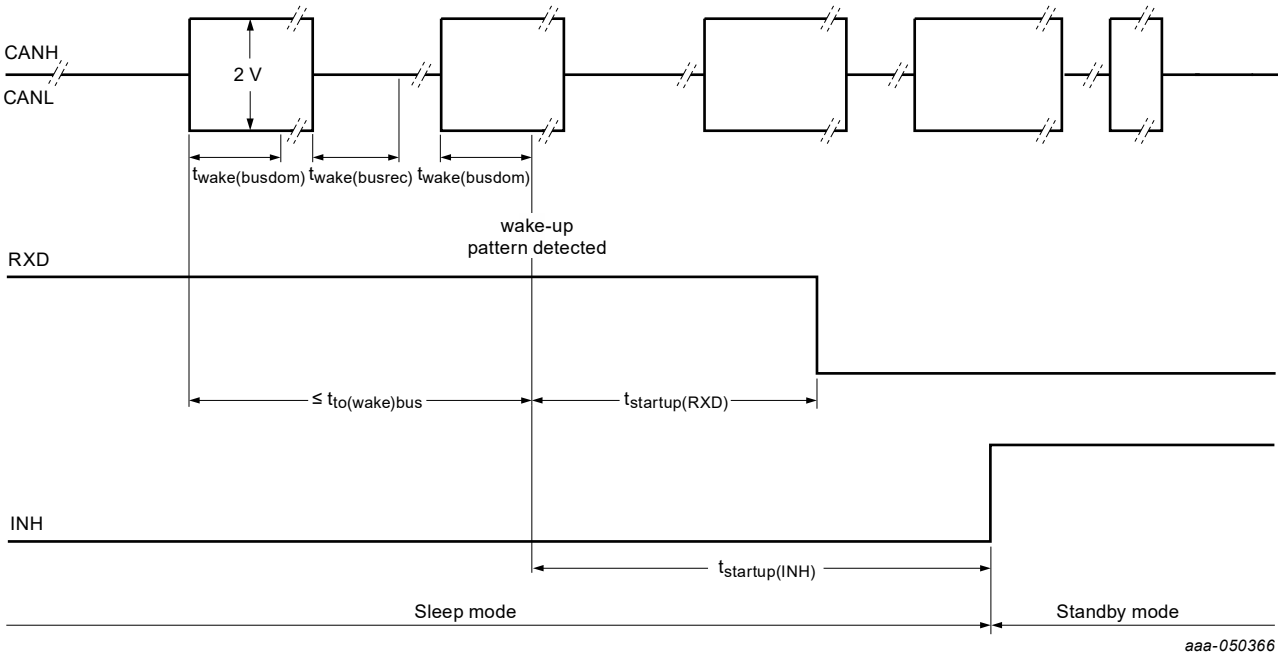


Figure 6. Standard wake-up pattern in Sleep mode with CWE = 1, PNCOK = 0 and CWC = 0

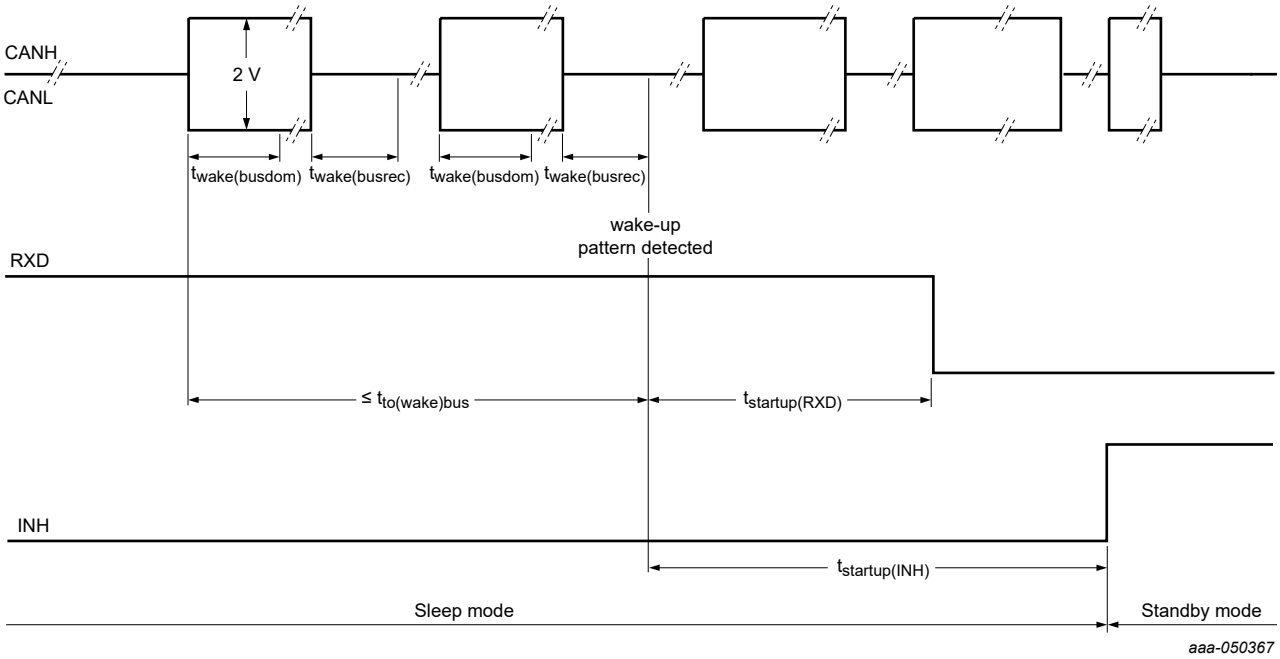


Figure 7. Extended wake-up pattern in Sleep mode with CWE = 1, PNCOK = 0 and CWC = 1

7.3.2.2 CAN wake-up frame (WUF)

CAN partial networking through selective wake-up detection allows a device in a CAN network to be selectively woken up in response to a wake-up frame (WUF) on the CAN bus.

Selective wake-up detection uses one of two filtering methods:

- Identifier-only filtering (PNDM = 0)
- Identifier + data length code + data mask filtering (PNDM = 1)

The following conditions must be met to enable CAN WUF functionality:

- CAN biasing needs to be activated (CAN OfflineBias, CAN ListenOnly or CAN Active mode)
- CAN wake-up enabled (CWE = 1)
- CAN partial networking configuration completed (PNCOK = 1)
- CAN partial networking enabled (CPNC = 1)
- No CAN partial networking error detected (CPNERRS = 0)

The PN configuration is defined in the following registers:

- ID registers (Table 29)
- ID mask registers (Table 30)
- Data mask registers (Table 31)
- Frame control register (Table 32)
- Data rate and filter configuration register (Table 33)

Bit PNCOK in the partial networking and CAN configuration register (Table 34) must be set (to 1) to activate the contents of the PN registers. PNCOK is cleared automatically when the contents of any PN register is changed and needs to be set again to load and activate the new configuration.

The arbitration bit rate is selected via bits CDR (see Table 33). CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s, 667 kbit/s and 1000 kbit/s are supported during selective wake-up.

7.3.2.2.1 Identifier matching

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the frame control register (Table 32).

- IDE = 0: standard CBFF (classical base frame format, 11-bit)
- IDE = 1: extended CEFF (classical extended frame format, 29-bit)

A valid WUF identifier is defined and stored in the ID registers (Table 29). An ID mask can be defined to exclude selected bits from being evaluated during WUF detection. The ID mask is defined in the mask registers (Table 30), where a 1 means ‘don’t care’.

When PNDM = 0, a valid wake-up frame is detected and a wake-up event is captured (CAN wake-up interrupt generated; see Table 40) when:

- the identifier field in the received wake-up frame matches the pattern in the PN ID registers (excluding the masked bits)
- the frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2024 (including CRC and CRC delimiter)

7.3.2.2.2 Data field matching

In addition to the identifier field, the data field in the CAN frame is also evaluated during WUF detection when PNDM = 1.

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the frame control register; Table 32) determines the number of data bytes expected (between 0 and 8) in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 31) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

The relationship between the data mask registers and the data bytes in the CAN message is illustrated in Figure 8. DM7 represents the mask for the last transmitted byte, DM6 for the last-but-one byte and so on.

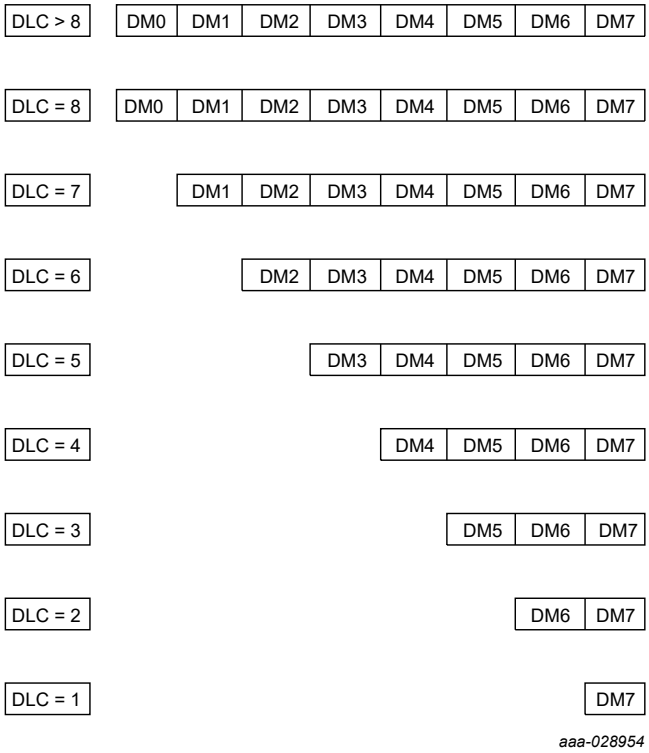


Figure 8. Data mask register usage for different values of DLC

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask (the data field is not evaluated when DLC = 0000). If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see Table 31). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

Remote frames do not contain data, but request data and can have a DLC ≠ 0000; so remote frames are not supported when PNDM = 1. If remote frames need to trigger a wake-up, identifier-only filtering should be selected (PNDM = 0).

When PNDM = 1, a WUF is detected when all the following conditions are met:

- The identifier field in the received wake-up frame matches the pattern and format in the ID registers (Table 29), excluding masked bits.
- The received CAN frame is not a Remote frame.
- The received data length code matches the DLC setting in the frame control register (Table 32).
- DLC:
  - DLC = 0000 or
  - DLC ≠ 0000 and at least one bit in the data field of the received frame is set with the corresponding bit in the associated data mask register (Table 31) also set.
- The frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2024 (including CRC and CRC delimiter).

7.3.2.2.3 WUF error processing

If the TJA1465 receives a CAN message containing a protocol error (e.g. a 'stuffing error') transmitted in advance of the ACK field, an internal error counter is incremented. If a classical CAN message (CBFF or CEFF) is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the CAN wake-up frame detector module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDER = 1) and the device wakes up.

The error counter value can be read via bits PN_ERR_ERROR_COUNT (Table 28). The counter is reset to zero when no activity is detected on the CAN bus for $t_{to(silence)}$ or selective wake-up detection is disabled (CPNC = 0 OR PNCOK = 0). The status, whether the last frame was decoded successfully, can be determined via bit LFDS in the partial networking status register (Table 27).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured (PNCOK = 0), wake-up will be performed as described in Section 7.3.2.1.

7.3.2.2.4 CAN FD passive and CAN XL passive

CAN frames in the ISO 11898-1:2024 compliant FD base frame format (FBFF) or FD extended frame format (FEFF), or the upcoming CAN XL frame format (XLFF), are not supported for selective wake-up. The device can be configured to tolerate these frames or treat them as invalid frames via bit PNECC in the partial networking control register (Table 34).

With PNECC = 0, the error counter is incremented when an FBFF, FEFF or XLFF frame is received. With PNECC = 1, the error counter is not affected because FBFF, FEFF and XLFF frames are ignored.

CAN FD tolerance as described in the ISO 11898-2 standard is supported for bitfilter 1 and bitfilter 2. The TJA1465 also supports additional bit filter settings for higher arbitration rates up to 1 Mbit/s and data bit rates up to 8 Mbit/s (see bits CDR and IDFS in Table 33 and $t_{fltr(bit)dom}$ in Table 50).

For CAN XL FAST mode (ISO 11898-2:2024) tolerance, CAN XL level-scheme detection must be enabled to prevent the new CAN XL voltage scheme being misinterpreted as bus idle. CAN XL FAST mode tolerance is enabled by setting CXLDE to 1.

7.4 Interrupt processing

A number of events can be captured and reported to the host via the interrupt mechanism. Pin RXD is used to signal an interrupt event in Standby or Sleep mode. Two options are supported:

- RXDINTC = 0: RXD goes LOW when a wake-up or power-on interrupt is pending
- RXDINTC = 1: RXD goes LOW when any interrupt is pending

Interrupts are enabled individually via dedicated bits in the interrupt enable registers (see Section 7.10.10). When an interrupt is generated, pin RXD goes LOW to alert the host. The host can then determine which event

triggered the interrupt by polling the interrupt status registers. PO and PNFDER interrupts are always enabled; so they do not have associated interrupt enable bits.

Interrupts are cleared by writing 1 (W1C) to the relevant interrupt status bits. Clearing an interrupt does not necessarily mean the event that triggered the interrupt has been resolved. If there is a collision, setting the interrupt takes precedence over clearing the interrupt.

7.5 Device ID

A byte is reserved in the register map for the unique device identification code; see bit IDS in Table 46.

7.6 Lock control

Sections of the register address area can be write-protected to prevent unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the TJA1465 updating registers. Sections that can be locked are detailed in Section 7.10.11.

7.7 General-purpose memory

The TJA1465 allocates 4 bytes of memory to store user information. The general-purpose registers can be accessed via the SPI at address 0xFF0 to 0xFF3 (see Section 7.10.12). The general-purpose registers are only cleared when the battery is first connected.

7.8 GPIO pins - TJA1465B only

The TJA1465B contains three general-purpose I/O pins (GPIO) that can be assigned to a number of functions (see Table 14 and Table 24 to Table 26).

Table 14. Configurable GPIO functions

GPIO function	Description
Digital input	pin status can be read via GPIOxS
Digital output	output polarity defined via GPPx
TXEN_N input	CAN transmitter disabled when GPIO pin driven HIGH
INT_N interrupt output	active state signals an interrupt is pending
Additional RXD output (RXD2)	GPIO1 only, two options: • CAN bus forwarded to both RXD and RXD2 (via GPIO1) outputs • CAN bus forwarded to RXD2 only; RXD forced HIGH in Listen Only and Normal modes; pin RXD behavior in all other modes as in Table 9
Additional TXD input (TXD2)	GPIO2 only, two options: • TXD and TXD2 (via GPIO2) data fed to the CAN bus - the CAN bus will be recessive only when both TXD and TXD2 are HIGH • only TXD2 enabled (TXD input ignored) - the CAN bus is driven dominant when TXD2 is LOW
V_{CC} undervoltage status output	active state indicates V_{CC} undervoltage detected (UVCCS)
TXD dominant status output	active state indicates TXD clamped dominant (TXDDOMS)
TXD2 dominant status output	active state indicates TXD2 clamped dominant (TXD2DOMS) - GPIO1 and GPIO3 only
CAN WUP detect status output	active state indicates WUP detected
CAN WUF detect status output	active state indicates WUF detected

Table 14. Configurable GPIO functions *...continued*

GPIO function	Description
CAN bus biasing status output	active state indicates bus biasing is active
WAKE pin rising edge detect output	active state indicates rising edge detected on WAKE pin
WAKE pin falling edge detect output	active state indicates falling edge detected on WAKE pin
CAN in Active mode and ready to transmit status output (CTS)	active state if CAN in Active mode
CAN in ListenOnly mode status output	active state if CAN in ListenOnly mode
Local low-voltage wake-up input	wake-up on rising, falling or both edges on GPIO pin
INH2: low-voltage inhibit output	active state if INH2 activated

The status of the GPIO pins, HIGH or LOW, can be read (after $t_{fltr(GPIO)}$) via bits GPIOxS in the GPIO status register (Table 23), independently of the selected function.

When an input function is selected, the pin behavior can be configured as:

- floating
- pull-up
- pull-down
- repeater

When an output function is selected, the pin output driver can be configured as:

- push-pull
- open-drain high-side driver
- high-side driver plus weak pull-down
- open-drain low-side driver
- low-side driver plus weak pull-up

For selected output functions, the GPIO pins can be configured as active-HIGH or active-LOW (see Table 22). The minimum pulse width when GPIO is configured as output is greater than $t_{w(min)}$.

7.9 Failure handling

The TJA1465 incorporates a number of safety features used for error detection and processing.

7.9.1 TXD dominant timeout

A LOW level on pin TXD (or on GPIO2 in TJA1465B when configured as a second TXD input, see Section 7.8) persisting longer than $t_{to(dom)TXD}$ releases the bus lines to recessive state. This feature prevents the CAN bus being blocked by continuous dominant clamping. A CAN failure interrupt is generated (TXDDOM/TXD2DOM = 1), if enabled (TXDDOME/TXD2DOME = 1), when a TXD dominant timeout is detected. The TXD dominant status can be read via bit TXDDOMS/TXD2DOMS in the CAN status register (Table 21).

7.9.2 CAN transmitter enable/disable(TXEN_N) - TJA1465B only

On the TJA1465B, the CAN transmitter can be enabled/disabled via the TXEN_N input. The GPIO pins can be configured as additional transmitter enable/disable signals (see Section 7.8). A HIGH level on pin TXEN_N, or on a GPIO pin configured as a TXEN_N input, disables the transmitter, releasing the bus lines to recessive state independent of the level on pin TXD and/or TXD2 (if configured on GPIO2). The TXEN_N status can be read via bit GPIO1S, GPIO2S and GPIO3S in the GPIO status register (Table 23).

7.9.3 Bus dominant timeout

A dominant state on the CAN bus lasting longer than $t_{to(dom)bus}$ generates a CAN bus failure interrupt (BUSDOM = 1), if enabled (BUSDOME = 1; Table 38). The status of the bus can be read via bit BUSDOMS in the CAN status register (Table 21). Note that this feature is only available in Normal mode and in Listen Only modes when LPL = 0.

7.9.4 V_{CC} undervoltage

The TJA1465 monitors the supply voltage on pin VCC. When V_{CC} drops below the undervoltage detection threshold $V_{uvd(VCC)}$ for longer than $t_{det(uv)}$, a V_{CC} undervoltage interrupt is generated (UVCC = 1), if enabled (UVCCE = 1; Table 37). The V_{CC} undervoltage status can be read via bit UVCCS in the system status register (Table 18).

7.9.5 V_{IO} undervoltage

The TJA1465 monitors the supply voltage on pin VIO. When V_{IO} drops below the undervoltage detection threshold $V_{uvd(VIO)}$ for longer than $t_{det(uv)long}$, the device switches to Sleep mode by setting mode control bits MC to Sleep. Pending wake-up interrupts are cleared and the wake-up sources are enabled (bits CWE, WPRE and WPFE set). The TJA1465 then waits for a wake-up request.

A long VIO undervoltage interrupt is generated (LUVIO = 1), if enabled (LUVIOE = 1; see Table 18). On recovering from an undervoltage event, the TJA1465 switches back to the selected mode (MC). Note that a long undervoltage event on VIO (LUVIO) will not be captured in Sleep mode.

The long undervoltage detection time, $t_{det(uv)long}$, is selected via bit LUVIOSEL in the system configuration register (Table 19).

7.9.6 V_{BAT} undervoltage

The TJA1465 monitors the supply voltage on pin VBAT. It switches directly to Off mode when V_{BAT} drops below the undervoltage detection threshold, $V_{uvd(VBAT)}$ for $t_{det(uv)}$. As a consequence, bit PO is set (see Table 40).

7.9.7 Overtemperature

The TJA1465 only monitors the junction temperature when MC = Normal. When the junction temperature exceeds $T_{j(sd)}$, the device switches from Normal mode to ListenOnly mode (see Section 7.2). An overtemperature interrupt is generated (OT = 1), if enabled (OTE = 1; see Table 40). The device recovers and switches back to Normal mode when the junction temperature falls below the shutdown release threshold, $T_{j(sd)rel}$. The overtemperature status can be read via bit OTS in the system status register (Table 18) when the device is in Normal or ListenOnly mode.

7.9.8 MCU reaction timeout

When the TJA1465 enters Standby mode from Sleep mode due to a wake-up or from Check_SNM mode, the MCU reaction timeout timer is started.

If a valid SPI frame is detected within $t_{to(MCU)}$, the MCU reaction timer is reset. If a valid SPI frame is not detected within $t_{to(MCU)}$, an MCU reaction timeout is triggered and the device switches to Sleep mode by setting mode control bits MC to Sleep. Pending wake-up interrupts are cleared and the wake-up sources are enabled (bits CWE, WPRE and WPFE set). The TJA1465 then waits for a wake-up request.

The MCU reaction timeout time depends on the long undervoltage threshold, selected via bit LUVIOSEL in the system configuration register (Table 19 and Table 50).

7.10 SPI interface

The serial peripheral interface (SPI) provides the communication link with the microcontroller. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 9.

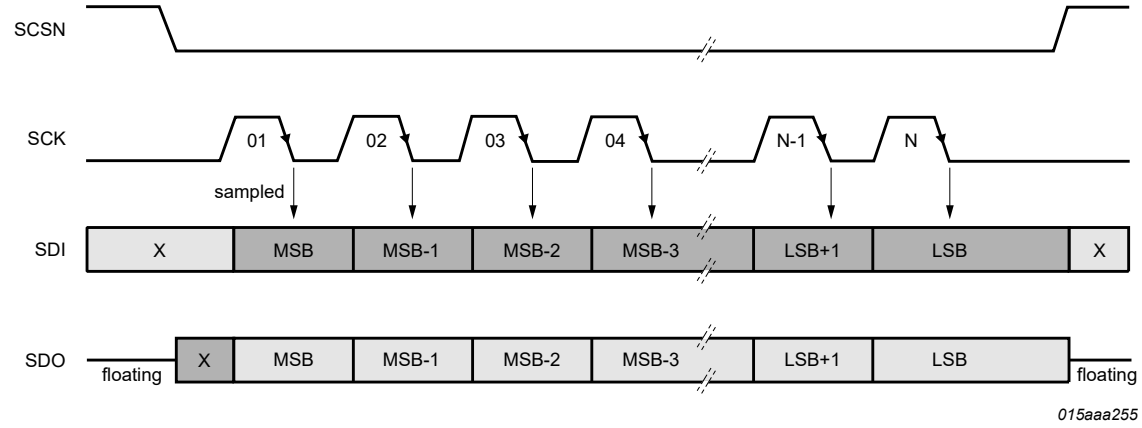


Figure 9. SPI timing protocol

The SPI data in the TJA1465 is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 12-bit address. A minimum of three bytes (24 bits) must be transmitted to the TJA1465 for a single register read or write operation (see Figure 9). Six bytes (48 bits) are needed to transmit the maximum of 4 data bytes (see Figure 10).

The first byte contains the 8 most significant bits of the address; the second byte contains the 4 least significant bits of the address, a ‘read-only’ bit, a 2-bit payload size (PLS) and a parity bit. The read-only bit must be 0 to indicate a write operation and 1 to indicate a read operation. PLS indicates the number of data bytes being transmitted:

- 00 - 1 data byte
- 01 - 2 data bytes
- 10 - 3 data bytes
- 11 - 4 data bytes

The parity bit covers the address bits, read-only bit and PLS bits. It must be calculated in the user application as part of the SPI command indicating even parity, creating an even number of 1s in the first 2 bytes including the parity bit.

The third and subsequent bytes contain the data to be written. For two or more data bytes (PLS ≠ 00), the register address is incremented automatically after each data byte, see Figure 10.

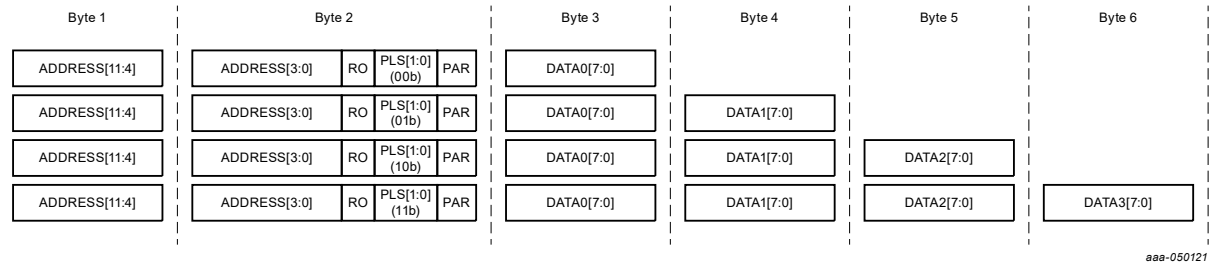


Figure 10. SPI addressing

During the SPI data, read or write operation, the first 15 bits received on pin SDI are returned via pin SDO; bit 16 returns the parity calculated for these 15 bits. During the data phase of the SPI protocol, the contents of the addressed register is returned via the SDO pin.

The devices tolerates write attempts to registers that do not exist.

7.10.1 SPI error handling

The TJA1465 can detect a number of SPI transmission failures:

- an incorrect parity bit was received
- the number of clock cycles is less than 24 or does not match the expected value based on the PLS
- an address rollover (> FFFh) was detected
- an undefined MC code was received
- a write access was attempted to a locked register
- the SPI message was not completed (SCSN HIGH) within the timeout time, $t_{to(SPI)}$

In all cases, an SPI fail interrupt is generated (provided SPIFE = 1) and the entire message is ignored.

When the necessary conditions for a Sleep mode transition (no wake-up source enabled or pending wake-up interrupt) are not met, the device will not switch to sleep mode, even though MC = 0001.

In the case of an incorrect parity or too many clock cycles, pin SDO goes LOW until the next rising edge on SCSN. When the duration of the SPI message exceeds $t_{to(SPI)}$, the SDO pin goes high-Z.

7.10.2 SPI system reset

A system reset can be forced via the SPI, causing the device to restart via Boot mode and setting bit PO. To trigger a system reset, enable SPI write access to the System reset register by setting LKRST to 0 in the Lock control register; then write consecutively 0x01 followed 0x80 to bits SFR in the System reset register (see Table 35). Both SPI accesses to the System reset register should be 24-bit. Any deviation from this sequence will abort the system reset.

Information that was in the general-purpose memory (Table 45) when the reset was initiated will still be available after the reset sequence has been completed.

7.10.3 SPI register map

Table 15. SPI register map overview

Register type	Address	Register name
Mode control	0x000	Mode control register
Interrupt enable (LKIE)	0x010	System interrupt enable register
	0x011	CAN interrupt enable register
	0x012	GPIO interrput enable register - TJA1465B only
Partial networking (LKPNC)	0x020	Partial networking ID register 0
	0x021	Partial networking ID register 1
	0x022	Partial networking ID register 2
	0x023	Partial networking ID register 3
	0x024	Partial networking ID mask register 0
	0x025	Partial networking ID mask register 1
	0x026	Partial networking ID mask register 2
	0x027	Partial networking ID mask register 3
	0x028	Partial networking data mask register 0
	0x029	Partial networking data mask register 1
	0x02A	Partial networking data mask register 2
	0x02B	Partial networking data mask register 3
	0x02C	Partial networking data mask register 4
	0x02D	Partial networking data mask register 5
	0x02E	Partial networking data mask register 6
	0x02F	Partial networking data mask register 7
	0x030	Partial networking frame control register
	0x031	Partial networking data rate and filter configuration register
	0x032	Partial networking and CAN configuration register
Configuration (LKCFG)	0x040	Wake-up pulse configuration register
	0x041	CAN configuration register
	0x042	GPIO1 configuration register - TJA1465B only
	0x043	GPIO2 configuration register - TJA1465B only
	0x044	GPIO3 configuration register - TJA1465B only
	0x045	GPIO polarity configuration register - TJA1465B only
	0x046	System configuration register
Lock	0x050	Lock control register
Interrupt status	0x060	System interrupt status register
	0x061	CAN interrupt status register
	0x062	Partial networking interrupt status register
	0x063	GPIO interrupt status register - TJA1465B only

Table 15. SPI register map overview...*continued*

Register type	Address	Register name
General status	0x070	Mode status register
	0x071	System status register
	0x072	CAN status register
	0x073	Partial networking status register
	0x074	GPIO/TXEN_N status register - TJA1465B only
	0x075	Partial networking error count status register
Reset (LKRST)	0xFE0	System reset register
General-purpose memory (LKGPM)	0xFF0	General-purpose memory register 0
	0xFF1	General-purpose memory register 1
	0xFF2	General-purpose memory register 2
	0xFF3	General-purpose memory register 3
ID	0xFFF	Device identification

7.10.4 System control and status registers

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Table 16. Mode control register (address 000h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3:0	MC	R/W	0001[1]	Sleep mode
			0110*	Standby mode
			1000	ListenOnly mode
			1111[2]	Normal mode

[1] Value when Sleep mode is entered due to expiration of VIO_UV_LONG or MCU_REAC_EXP.
[2] Value after Check_SNM-to-Normal mode transition

Table 17. Mode status register (address 070h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3:0	MCS	R	0001	Sleep mode
			0110	Standby mode
			1000	ListenOnly mode
			1111	Normal mode

Table 18. System status register (address 071h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	ignore on read

Table 18. System status register (address 071h)*...continued*

Bit	Symbol	Access	Value	Description
6	FSMS	R		most recent Sleep mode transition:
			0	triggered by SPI
			1	triggered by VIO undervoltage or MCU timeout
5	OTS	R		overtemperature status available when MC = Normal and MCS = Normal/Listen Only
			0	no overtemperature or MC ≠ Normal
			1	overtemperature detected
4	reserved	R	-	ignore on read
3	UVCCS	R		V_{CC} undervoltage status
			0	no undervoltage on VCC
			1	V_{CC} undervoltage detected
2	NMS	R		Normal mode status
			0	device entered Normal mode after power up
			1	device did not enter Normal mode power up
1	SNMS	R		Start-to-Normal mode status
			0	device did not enter Normal mode after power up
			1	device entered Normal mode directly from Check_SNM mode
0	WPS	R		WAKE pin status
			0	WAKE pin LOW
			1	WAKE pin HIGH

Table 19. System configuration register (address 046h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3	BCCTRL	R/W		VBAT clamp control:
			0*	enable VBAT clamp
			1	disable VBAT clamp
2	RXDINTC	R/W		interrupt signaling at RXD in Sleep/Standby modes
			0*	wake-up and power-on interrupts detected
			1	all enabled interrupts detected
1	LUVIOSEL	R/W		long VIO undervoltage detection time and MCU reaction timeout time select
			0	$t_{det(uv)long1}$, $t_{to(MCU)1}$
			1*	$t_{det(uv)long2}$, $t_{to(MCU)2}$
0	VBATVCC	R/W		VBAT/VCC configuration
			0*	separate V_{BAT} and V_{CC} supplies; typical application; autobiasing supplied from V_{BAT}

Table 19. System configuration register (address 046h)*...continued*

Bit	Symbol	Access	Value	Description
			1	common V_{BAT} and V_{CC} supplies; applications with permanently active regulator; autobiasing is supplied from V_{CC}

7.10.5 CAN configuration and status registers

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Table 20. CAN configuration register (address 041h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	always write 00; ignore on read
5	TXRXLP	R/W		TXD-to-RXD loopback:
			0*	normal TXD and RXD behavior
			1	TXD is forwarded to RXD and CAN bus remains recessive in CAN Active mode
4	reserved: *TJA1465A*	R	-	always write 0; ignore on read
4	TX2RX2LP[1] *TJA1465B*	R/W		TXD2-to-RXD2 loopback:
			0*	normal TXD2 and RXD2 behavior
			1	TXD2 is forwarded to RXD2 and CAN bus remains recessive in CAN Active mode
3:2	reserved	R	-	always write 00; ignore on read
1	LPL	R/W		low-power ListenOnly mode enable:
			0*	low-power ListenOnly mode disabled
			1	low-power ListenOnly mode enabled
0	CWC	R/W		CAN wake-up pattern selection:
			0*	ISO 11898-2:2024 wake pattern (dom-rec-dom)
			1	ISO 11898-2:2024 wake pattern (dom-rec-dom-rec)

[1] GPIO1 configured as second RXD output (RXD2) and GPIO2 configured as second TXD input (TXD2).

Table 21. CAN status register (address 072h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode or not ready to transmit
			1	CAN transceiver in Active mode and ready to transmit
6:4	reserved	R	-	ignore on read
3	CBSS	R		CAN bus silence status:
			0	no bus silence longer than $t_{to(silence)}$ detected
			1	bus silence detected for longer than $t_{to(silence)}$

Table 21. CAN status register (address 072h)*...continued*

Bit	Symbol	Access	Value	Description
2	BUSDOMS	R		BUS clamped dominant status:
			0	CAN bus not clamped dominant
			1	CAN bus clamped dominant
1	reserved: *TJA1465A*	R	-	ignore on read
1	TXD2DOMS *TJA1465B*	R		TXD2 clamped dominant status:
			0	TXD2 not clamped dominant
			1	TXD2 clamped dominant
0	TXDDOMS	R		TXD clamped dominant status:
			0	TXD not clamped dominant
			1	TXD clamped dominant

7.10.6 GPIO configuration and status registers: TJA1465B only

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Table 22. GPIO output polarity configuration register (address 045h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	always write 00000; ignore on read
2	GPP3	R/W		GPIO3 polarity:
			0*	default polarity
			1	inverted polarity
1	GPP2	R/W		GPIO2 polarity:
			0*	default polarity
			1	inverted polarity
0	GPP1	R/W		GPIO1 polarity:[1]
			0*	default polarity
			1	inverted polarity

[1] n.a when when GPIO1 is configured as RXD2.

Table 23. GPIO/TXEN_N status register (address 074h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3	TXENS	R		TXEN_N pin status:
			0	TXEN_N LOW
			1	TXEN_N HIGH
2	GPIO3S	R		GPIO3 pin status:
			0	GPIO3 LOW

Table 23. GPIO/TXEN_N status register (address 074h)*...continued*

Bit	Symbol	Access	Value	Description
			1	GPIO3 HIGH
1	GPIO2S	R		GPIO2 pin status:
			0	GPIO2 LOW
			1	GPIO2 HIGH
0	GPIO1S	R		GPIO1 pin status:
			0	GPIO1 LOW
			1	GPIO1 HIGH

Table 24. GPIO1 configuration register (address 042h)

Bit	Symbol	Access	Value	Description
7:5	GPIO1C	R/W		GPIO1 pin configuration:
			000	input: floating output: push-pull
			001	input: pull-up output: open-drain high-side driver
			010	input: pull-down output: high-side driver plus weak pull-down
			011*	input: repeater output: open-drain low-side driver
			100	input: repeater output: low-side driver plus weak pull-up
			101 - 111	reserved
4:0	GPIO1FS	R/W		GPIO1 function select:
			0x00*	repeater function active, independent of GPIO1C
			0x01	digital input
			0x02	digital output: LOW when GPP1 = 0; HIGH when GPP1 = 1
			0x03	TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH
			0x04	INT_N interrupt output; active-LOW when GPP1 = 0 (default); active-HIGH when GPP1 = 1
			0x05	reserved
			0x06	GPIO1 configured as second RXD output (RXD2); CAN bus forwarded to both GPIO1 (RXD2) and RXD
			0x07	reserved
			0x08	GPIO1 configured as second RXD output (RXD2); CAN bus only forwarded to GPIO1 (RXD2)
			0x09	V_{CC} undervoltage status output (UVCCS)[1]
			0x0A	TXD dominant status output (TXDDOMS)[1]

Table 24. GPIO1 configuration register (address 042h)*...continued*

Bit	Symbol	Access	Value	Description
			0x0B	TXD2 dominant status output (TXD2DOMS; available when GPIO2 configured as TXD2)[1]
			0x0C	wake-up pattern detect output[1]
			0x0D	wake-up frame detect output[1]
			0x0E	CAN bus biasing status output (HIGH, by default, indicates that CAN bus biasing is active)[1]
			0x0F	WAKE pin rising edge detect output[1]
			0x10	WAKE pin falling edge detect output[1]
			0x11	CAN Active mode ready-to-transmit status output (CTS)[1]
			0x12	CAN ListenOnly mode status output[1]
			0x13	digital input, rising edge qualified for wake-up interrupt if enabled via GPIO1E
			0x14	digital input, falling edge qualified for wake-up interrupt if enabled via GPIO1E
			0x15	digital input, rising and falling edge qualified for wake-up interrupt if enabled via GPIO1E
			0x16	INH2 output[1]
			0x17 to 0x1F	reserved

[1] Active-HIGH when GPP1 = 0; active-LOW when GPP1 = 1

Table 25. GPIO2 configuration register (address 043h)

Bit	Symbol	Access	Value	Description
7:5	GPIO2C	R/W		GPIO2 pin configuration:
			000	input: floating output: push-pull
			001	input: pull-up output: open-drain high-side driver
			010	input: pull-down output: high-side driver plus weak pull-down
			011*	input: repeater output: open-drain low-side driver
			100	input: repeater output: low-side driver plus weak pull-up
			101 - 111	reserved
4:0	GPIO2FS	R/W		GPIO2 function select:
			0x00*	repeater function active, independent of GPIO2C
			0x01	digital input
			0x02	digital output: LOW when GPP2 = 0; HIGH when GPP2 = 1
			0x03	TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH

Table 25. GPIO2 configuration register (address 043h)*...continued*

Bit	Symbol	Access	Value	Description
			0x04	INT_N interrupt output; active-LOW when GPP2 = 0 (default); active-HIGH when GPP2 = 1
			0x05	GPIO2 configured as second TXD input (TXD2); TXD and TXD2 (via GPIO2) data fed to the CAN bus
			0x06	reserved
			0x07	GPIO2 configured as second TXD input (TXD2); only TXD2 (via GPIO2) data fed to the CAN bus; TXD input ignored
			0x08	reserved
			0x09	V_{CC} undervoltage status output (UVCCS)[1]
			0x0A	TXD dominant status output (TXDDOMS)[1]
			0x0B	reserved
			0x0C	wake-up pattern detect output[1]
			0x0D	wake-up frame detect output[1]
			0x0E	CAN bus biasing status (HIGH, by default, indicates that CAN bus biasing is active)[1]
			0x0F	WAKE pin rising edge detect output[1]
			0x10	WAKE pin falling edge detect output[1]
			0x11	CAN Active mode ready-to-transmit status output (CTS)[1]
			0x12	CAN ListenOnly mode status[1]
			0x13	digital input, rising edge qualified for wake-up interrupt if enabled via GPIO2E
			0x14	digital input, falling edge qualified for wake-up interrupt if enabled via GPIO2E
			0x15	digital input, rising and falling edge qualified for wake-up interrupt if enabled via GPIO2E
			0x16	INH2 output[1]
			0x17 to 0x1F	reserved

[1] Active-HIGH when GPP2 = 0; active-LOW when GPP2 = 1

Table 26. GPIO3 configuration register (address 044h)

Bit	Symbol	Access	Value	Description
7:5	GPIO3C	R/W		GPIO3 pin configuration:
			000	input: floating output: push-pull
			001	input: pull-up output: open-drain high-side driver
			010	input: pull-down output: high-side driver plus weak pull-down
			011*	input: repeater output: open-drain low-side driver

Table 26. GPIO3 configuration register (address 044h)*...continued*

Bit	Symbol	Access	Value	Description
			100	input: repeater output: low-side driver plus weak pull-up
			101 - 111	reserved
4:0	GPIO3FS	R/W		GPIO3 function select:
			0x00*	repeater function active, independent of GPIO3C
			0x01	digital input
			0x02	digital output: LOW when GPP3 = 0; HIGH when GPP3 = 1
			0x03	TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH
			0x04	INT_N interrupt output; active-LOW when GPP3 = 0 (default); active-HIGH when GPP3 = 1
			0x05	reserved
			0x06	reserved
			0x07	reserved
			0x08	reserved
			0x09	V_{CC} undervoltage status output (UVCCS)[1]
			0x0A	TXD dominant status output (TXDDOMS)[1]
			0x0B	TXD2 dominant status output (TXD2DOMS; available when GPIO2 configured as TXD2)[1]
			0x0C	wake-up pattern detect output[1]
			0x0D	wake-up frame detect output[1]
			0x0E	CAN bus biasing status (HIGH, by default, indicates that CAN bus biasing is active)[1]
			0x0F	WAKE pin rising edge detect output[1]
			0x10	WAKE pin falling edge detect output[1]
			0x11	CAN Active mode ready-to-transmit status output (CTS)[1]
			0x12	CAN ListenOnly mode status[1]
			0x13	digital input, rising edge qualified for wake-up interrupt if enabled via GPIO3E
			0x14	digital input, falling edge qualified for wake-up interrupt if enabled via GPIO3E
			0x15	digital input, rising and falling edge qualified for wake-up interrupt if enabled via GPIO3E
			0x16	INH2 output[1]
			0x17 to 0x1F	reserved

[1] Active-HIGH when GPP3 = 0; active-LOW when GPP3 = 1

7.10.7 Partial networking registers

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '#'.

Table 27. Partial networking status register (address 073h)

Bit	Symbol	Access	Value	Description
7	SYNCS	R		CAN partial networking sync status:
			0	CAN partial networking core not ready to decode frame
			1	CAN partial networking core ready to decode frame
6	CPNERRS	R		CAN partial networking error status:
			0	no CAN partial networking error detected; PNFDER = 0 and PNCOK = 1
			1	CAN partial networking error detected; PNFDER =1 or PNCOK = 0; wake-up via WUP only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected; PNCOK = 0
			1	CAN partial networking configuration OK; PNCOK = 1
4	LFDS	R		last frame decode status:
			0	most recent CAN frame not decoded successfully
			1	most recent CAN frame decoded successfully
3:0	reserved	R	-	ignore on read

Table 28. Partial networking error count status register (address 075h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	ignore on read
4:0	PNERRCNT	R		CAN partial networking error count status:
			00000	0
			00001	1
			00010	2
			00011	3
			...	...
			11111	31

Table 29. Partial networking ID registers 0 to 3 (addresses 020h to 023h)

Addr.	Bit	Symbol	Access	Value	Description
020h	7:0	ID7:ID0	R/W	00h#	bits ID7 to ID0 of the extended frame format
021h	7:0	ID15:ID8	R/W	00h#	bits ID15 to ID8 of the extended frame format
022h	7:2	ID23:ID18	R/W	00h#	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	00h#	bits ID17 to ID16 of the extended frame format

Table 29. Partial networking ID registers 0 to 3 (addresses 020h to 023h)*...continued*

Addr.	Bit	Symbol	Access	Value	Description
023h	7:5	reserved	R	-	always write 000; ignore on read
	4:0	ID28:ID24	R/W	00h#	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 30. Partial networking ID mask registers 0 to 3 (addresses 024h to 027h)

Addr.	Bit	Symbol	Access	Value	Description
024h	7:0	M7:M0	R/W	00h#	ID mask bits 7 to 0 of extended frame format
025h	7:0	M15:M8	R/W	00h#	ID mask bits 15 to 8 of extended frame format
026h	7:2	M23:M18	R/W	00h#	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	00h#	ID mask bits 17 to 16 of extended frame format
027h	7:5	reserved	R/W	00h#	always write 000; ignore on read
	4:0	M28:M24	R/W	00h#	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 31. Partial networking data mask registers 0 to 7 (addresses 028h to 02Fh)

Addr.	Bit	Symbol	Access	Value	Description
028h	7:0	DM0	R/W	FFh#	data mask 0 configuration
029h	7:0	DM1	R/W	FFh#	data mask 1 configuration
02Ah	7:0	DM2	R/W	FFh#	data mask 2 configuration
02Bh	7:0	DM3	R/W	FFh#	data mask 3 configuration
02Ch	7:0	DM4	R/W	FFh#	data mask 4 configuration
02Dh	7:0	DM5	R/W	FFh#	data mask 5 configuration
02Eh	7:0	DM6	R/W	FFh#	data mask 6 configuration
02Fh	7:0	DM7	R/W	FFh#	data mask 7 configuration

Table 32. Partial networking frame control register (address 030h)

Bit	Symbol	Access	Value	Description
7	IDE	R/W		identifier format:
			0#	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W		partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1#	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	always write 00; ignore on read
3:0	DLC	R/W		number of data bytes expected in a CAN frame (DLC):

Table 32. Partial networking frame control register (address 030h)*...continued*

Bit	Symbol	Access	Value	Description
			0000#	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	8

Table 33. Partial networking data rate and filter configuration register (address 031h)

Bit	Symbol	Access	Value	Description
7:4	IDFS	R/W		idle detection filter select:
			0000#	bitfilter 0: ignore < 5.0 % of arbitration bit time; detect > 17.5 % of arbitration bit time (500 kbit/s max)
			0001	ISO bitfilter 1: ignore < 5.0 % of arbitration bit time; detect > 17.5 % of arbitration bit time (500 kbit/s max)
			0010	ISO bitfilter 2: ignore < 2.5 % of arbitration bit time; detect > 8.75 % of arbitration bit time (500 kbit/s max)
			0011	bitfilter 3: ignore < 18 ns; detect > 93 ns
			0100	bitfilter 4: ignore < 42 ns; detect > 119 ns
			0101	bitfilter 5: ignore < 67 ns; detect > 145 ns
			0110	bitfilter 6: ignore < 91 ns; detect > 170 ns
			0111 to 1111	reserved
3	reserved	R	-	always write 0; ignore on read
2:0	CDR	R/W		CAN arbitration bit rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100#	500 kbit/s
			101	667 kbit/s
			110	reserved (PNCORE disabled)
			111	1 Mbit/s

Table 34. Partial networking and CAN configuration register (address 032h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3	CXLDE	R/W		CAN XL FAST mode tolerance enable (used for bus integration):
			0#	CAN XL FAST mode tolerance disabled
			1	CAN XL FAST mode tolerance enabled
2	PNECC	R/W		partial networking error counter control:
			0#	CAN XL and CAN FD frames will increment error counter
			1	CAN XL and CAN FD frames will not increment error counter
1	PNCOK	R/W		CAN partial networking configuration:
			0#	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking register configuration valid
0	CPNC	R/W		CAN selective wake-up enable:
			0#	disable CAN selective wake-up
			1	enable CAN selective wake-up

7.10.8 System reset register

Table 35. System reset register (address FE0h)

Bit	Symbol	Access	Value	Description
7:0	SFR	W		software-forced system reset:
			01h	set up system reset
			80h	confirm system reset

7.10.9 Wake-up pulse configuration register

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Table 36. Wake-up pulse configuration register (address 040h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R	-	always write 00h; ignore on read
0	WFC	R/W		wake-up pulse width (t_{wake}) on WAKE pin
			0*	short wake-up time
			1	long wake-up time

7.10.10 Interrupt registers

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Write 1 to clear (W1C) interrupt status bit after interrupt detected.

Table 37. System interrupt enable register (address 010h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	always write 0; ignore on read
6	CWE	R/W		CAN wake-up interrupt enable:
			0*	disable CAN wake-up interrupt
			1[1]	enable CAN wake-up interrupt
5	OTE	R/W		overtemperature shutdown interrupt enable:
			0*	disable overtemperature shutdown interrupt
			1	enable overtemperature shutdown interrupt
4	SPIFE	R/W		SPI failure interrupt enable:
			0*	disable SPI failure interrupt
			1	enable SPI failure interrupt
3	UVCCE	R/W		V_{CC} undervoltage interrupt enable:
			0	disable V_{CC} undervoltage interrupt
			1*	enable V_{CC} undervoltage interrupt
2	LUVIOE	R/W		long V_{IO} undervoltage interrupt enable:
			0	disable long V_{IO} undervoltage interrupt
			1*	enable long V_{IO} undervoltage interrupt
1	WPRE	R/W		WAKE pin rising-edge interrupt enable:
			0*	disable WAKE pin rising-edge interrupt
			1[1]	enable WAKE pin rising-edge interrupt
0	WPFE	R/W		WAKE pin falling-edge interrupt enable:
			0*	disable WAKE pin falling-edge interrupt
			1[1]	enable WAKE pin falling-edge interrupt

[1] Value when Sleep mode is entered due to expiration of VIO_UV_LONG or MCU_REAC_EXP.

Table 38. CAN interrupt enable register (address 011h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3	CBSE	R/W		CAN bus silence interrupt enable:
			0*	disable CAN bus silence interrupt
			1	enable CAN bus silence interrupt

Table 38. CAN interrupt enable register (address 011h)*...continued*

Bit	Symbol	Access	Value	Description
2	BUSDOME	R/W		CAN bus dominant interrupt enable:
			0*	disable CAN bus dominant interrupt
			1	enable CAN bus dominant interrupt
1	reserved: *TJA1465A*	R	-	always write 0; ignore on read
1	TXD2DOME *TJA1465B*	R/W		TXD2 dominant timeout interrupt enable:
			0*	disable TXD2 dominant timeout interrupt
			1	enable TXD2 dominant timeout interrupt
0	TXDDOME	R/W		TXD dominant timeout interrupt enable:
			0*	disable TXD dominant timeout interrupt
			1	enable TXD dominant timeout interrupt

Table 39. GPIO interrupt enable register (address 012h) - TJA1465B only

For GPIOx wake-up detection, bits GPIOxFS must be set to 0x13, 0x14 or 0x15 (see Table 24 to Table 26).

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	always write 00000; ignore on read
2	GPIO3E	R/W		GPIO3 interrupt enable:
			0*	disable GPIO3 interrupt
			1	enable GPIO3 interrupt
1	GPIO2E	R/W		GPIO2 interrupt enable:
			0*	disable GPIO2 interrupt
			1	enable GPIO2 interrupt
0	GPIO1E	R/W		GPIO1 interrupt enable:
			0*	disable GPIO1 interrupt
			1	enable GPIO1 interrupt

Table 40. System interrupt status register (address 060h)

Bit	Symbol	Access	Value	Description
7	PO[1]	R/W1C		power-on/system reset interrupt:
			0	no power-on/system reset interrupt detected
			1*	power-on/system reset interrupt detected
6	CW[2]	R/W1C		CAN wake-up interrupt:
			0*	no CAN wake-up interrupt detected
			1	CAN wake-up interrupt detected
5	OT	R/W1C		overtemperature warning interrupt:
			0*	no overtemperature warning interrupt detected

Table 40. System interrupt status register (address 060h)*...continued*

Bit	Symbol	Access	Value	Description
			1	overtemperature warning interrupt detected
4	SPIF	R/W1C		SPI failure interrupt:
			0*	no SPI failure interrupt detected
			1	SPI failure interrupt detected
3	UVCC	R/W1C		V_{CC} undervoltage interrupt:
			0*	no V_{CC} undervoltage interrupt detected
			1	V_{CC} undervoltage interrupt detected
2	LUVIO	R/W1C		long V_{IO} undervoltage interrupt:
			0*	no long V_{IO} undervoltage interrupt detected
			1	long V_{IO} undervoltage interrupt detected
1	WPR[2]	R/W1C		WAKE pin rising-edge interrupt:
			0*	no WAKE pin rising-edge interrupt detected
			1	WAKE pin rising-edge interrupt detected
0	WPF[2]	R/W1C		WAKE pin falling-edge interrupt:
			0*	no WAKE pin falling-edge interrupt detected
			1	WAKE pin falling-edge interrupt detected

[1] PO interrupt is always enabled.
[2] This interrupt is also a wake-up source.

Table 41. CAN interrupt status register (address 061h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 1111; ignore on read
3	CBS	R/W1C		CAN bus silence interrupt:
			0*	no CAN bus silence interrupt detected
			1	CAN bus silence interrupt detected
2	BUSDOM	R/W1C		CAN bus dominant interrupt:
			0*	no CAN bus dominant interrupt detected
			1	CAN bus dominant interrupt detected
1	reserved: *TJA1465A*	R	-	always write 0; ignore on read
1	TXD2DOM *TJA1465B*	R/W1C		TXD2 dominant timeout interrupt:
			0*	no TXD2 dominant timeout interrupt detected
			1	TXD2 dominant timeout interrupt detected
0	TXDDOM	R/W1C		TXD dominant timeout interrupt:
			0*	no TXD dominant timeout interrupt detected
			1	TXD dominant timeout interrupt detected

Table 42. Partial networking interrupt status register (address 062h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	always write 11111; ignore on read
2	PNFDER[1]	R/W1C		partial networking frame detection error interrupt:
			0*	no partial networking frame detection error interrupt detected
			1	partial networking frame detection error interrupt detected
1:0	reserved	R	-	always write 11; ignore on read

[1] PNFDER interrupt is always enabled.

Table 43. GPIO interrupt status register (address 063h) - TJA1465B only>

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	always write 11111; ignore on read
2	GPIO3	R/W1C		GPIO3 interrupt:
			0*	no GPIO3 interrupt detected
			1	GPIO3 interrupt detected
1	GPIO2	R/W1C		GPIO2 interrupt:
			0*	no GPIO2 interrupt detected
			1	GPIO2 interrupt detected
0	GPIO1	R/W1C		GPIO1 interrupt:
			0*	no GPIO1 interrupt detected
			1	GPIO1 interrupt detected

7.10.11 Lock control register

Reset values after system startup (BOOT_OK; see Figure 4) are indicated by '*'.

Table 44. Lock control register (address 050h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	always write 000; ignore on read
4	LKGPM	R/W		Lock control: general-purpose memory registers (0xFF0 to 0xFF3):
			0*	SPI write access enabled
			1	SPI write access disabled
3	LKRST	R/W		Lock control: system reset register (0xFE0):
			0	SPI write access enabled
			1*	SPI write access disabled
2	LKCFG	R/W		Lock control: System/Wake/CAN configuration registers (0x40 to 0x46):
			0*	SPI write access enabled
			1	SPI write access disabled
1	LKPNC	R/W		Lock control: partial networking configuration registers (0x020 to 0x032):
			0*	SPI write access enabled

Table 44. Lock control register (address 050h)*...continued*

Bit	Symbol	Access	Value	Description
			1	SPI write access disabled
0	LKIE	R/W		Lock control: interrupt enable registers (0x010, 0x011, 0x012 - TJA1465B only):
			0*	SPI write access enabled
			1	SPI write access disabled

7.10.12 General-purpose memory registers

The TJA1465 allocates 4 bytes of memory for general-purpose registers used to store user information. Note that these registers are not cleared during an SPI system reset. They are cleared when the device enters Off mode.

Table 45. General-purpose memory registers 0 to 3 (addresses FF0h to FF3h)

Addr.	Bit	Symbol	Access	Value	Description
FF0h	7:0	GPM[7:0]	R/W	00h	general-purpose memory 0
FF1h	7:0	GPM[15:8]	R/W	00h	general-purpose memory 1
FF2h	7:0	GPM[23:16]	R/W	00h	general-purpose memory 2
FF3h	7:0	GPM[31:24]	R/W	00h	general-purpose memory 3

7.10.13 Device identification register

Table 46. Device identification register (address FFFh)

Bit	Symbol	Access	Value	Description
7:0	IDS	R		device identification number:
			10h	TJA1465A
			20h	TJA1465B

8 Limiting values

Table 47. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	Voltage on pin x[1]	pins VCC, VIO	-0.3	+6	V
			-	+7[2]	V
		pin VBAT	-	+40	V
		pin INH	-0.3	V_{BAT}+0.3[3]	V
		pins CANH, CANL, WAKE	-36	+40	V
		pins RXD, TXD, SCSN, SCK, SDI, SDO, TXEN_N, GPIOx	-0.3	V_{IO}+0.3[4]	V
$I_{r(VBAT)}$	reverse current on pin VBAT		-10	-	mA
$I_{O(INH)}$	output current on pin INH		-2	-	mA
$I_{O(TXEN\_N)}$	output current on pin TXEN_N		-	18	mA
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V
V_{trt}	transient voltage	on pin VBAT; on pins CANH, CANL and WAKE via 1 nF capacitor; pin WAKE with 3 kΩ resistor [5]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [6]			
		on pins CANH, CANL; on pin VBAT via 100 nF capacitor; on pin WAKE with ≥3 kΩ resistor	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [7]	-4	+4	kV
		on pins CANH, CANL [8]	-8	+8	kV
		Charged Device Model (CDM) [9]			
		on any pin	-500	+500	V
		on corner pins [10]	-750	+750	V
T_{vj}	virtual junction temperature	[11]	-40	+150	°C
T_{stg}	storage temperature	[12]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.
[3] Absolute maximum of 40 V.
[4] Subject to the qualifications detailed in Table notes 1 and 2 above for pin VIO, and for VIO-related pins.
[5] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637, part 2.

[6] Verified by an external test house according to IEC TS 62228, Section 4.3.
[7] According to AEC-Q100-002.
[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 15 and Figure 16). HBM pulse as specified in AEC-Q100-002 used.
[9] According to AEC-Q100-011.
[10] Only valid for TJA1465AT.
[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[12] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 48. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO14	85	K/W
		HVSON14	70	K/W
		DHVQFN18	68	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	HVSON14	33	K/W
		DHVQFN18	28	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO14	8	K/W
		HVSON14	11	K/W
		DHVQFN18	9	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).
[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 49. Static characteristics

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	4	-	4.5	V
V_{uvhys}	undervoltage hysteresis voltage		50	-	-	mV
I_{CC}	supply current	Normal mode; transmitter dominant	-	42	60	mA
		Normal mode; short circuit on bus lines; -3 V < (V_{CANH} = V_{CANL}) < +40 V	-	-	125	mA
		Normal mode, transmitter recessive	-	7	10	mA
		ListenOnly mode, LPL = 0	-	7	10	mA
		ListenOnly mode; LPL = 1; VBATVCC = 0; T_{vj} < 150 °C	-	-	40	µA
		ListenOnly mode; LPL = 1; VBATVCC = 1; T_{vj} < 150 °C	-	90	165	µA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	3	µA
		Standby or Sleep mode; T_{vj} < 150 °C	-	-	40	µA
I/O level adapter supply; pin VIO						
V_{IO}	supply voltage		1.71	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	1.5	-	1.71	V
V_{uvhys}	undervoltage hysteresis voltage		33	-	-	mV
I_{IO}	supply current	Normal or ListenOnly mode (excluding pull-up currents on V_{IO}-related pins); V_{TXD} = V_{IO}	-	-	5	µA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	2	µA
		Standby or Sleep mode; T_{vj} < 150 °C	-	-	4	µA
Supply; pin VBAT						
V_{BAT}	battery supply voltage		4.75	-	40	V
V_{uvd}	undervoltage detection voltage	all modes [2]	4.25	-	4.75	V
I_{BAT}	battery supply current	Normal mode or (ListenOnly mode; VBATVCC = 1 or LPL = 0); pin INH left open; CXLDE = 0; V_{BAT} ≤ 28 V [3]	-	-	400	µA
		ListenOnly mode; VBATVCC = 0 and LPL = 1; pin INH left open; CXLDE = 0; V_{BAT} ≤ 28 V [3]	-	-	525	µA

Table 49. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Sleep or Standby mode; CAN Offline Bias mode; pin INH left open; CXLDE = 0; CWE = 1; CPNC = 1; PNCOK = 1; $V_{WAKE} = V_{BAT}$; $V_{BAT} \leq 28$ V [3]				
		VBATVCC = 0; $T_{vj} < 85$ °C	-	-	450	µA
		VBATVCC = 0; $T_{vj} < 150$ °C	-	-	500	µA
		VBATVCC = 1; $T_{vj} < 85$ °C	-	-	350	µA
		VBATVCC = 1; $T_{vj} < 150$ °C	-	-	375	µA
		CXLDE = 1; additional battery current when CXLDE changes from 0 to 1 with CPNC = 1 and PNCOK = 1; all modes except Off and CAN Offline	-	55	110	µA
		Sleep or Standby mode; CAN Offline mode; pin INH left open; $V_{WAKE} = V_{BAT}$ or GND; $V_{BAT} \leq 28$ V				
		$T_{vj} < 85$ °C	-	12	20	µA
		$T_{vj} < 150$ °C	-	12	33	µA
		V_{BAT} = 32 V; BCCTRL = 0; additional current due to V_{BAT} being increased to 32 V		0.15	0.5	mA
		V_{BAT} = 40 V; BCCTRL = 0; additional current due to V_{BAT} being increased to 40 V		1.2	1.8	mA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
$I_{IL(off)}$	off state input leakage current	Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{TXD} < V_{IO}$	-5	-	+5	µA
C_i	input capacitance	[3]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	1	-	10	mA
$I_{IL(off)}$	off state input leakage current	Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{RXD} < V_{IO}$	-5	-	+5	µA
Inhibit output pin; pin INH						
ΔV_H	HIGH-level voltage drop	$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -1 mA	0	-	1	V
		$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -2 mA	0	-	2	V

Table 49. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_L	leakage current	Sleep mode; Off mode	-2	-	+2	µA
$I_{O(sc)}$	short-circuit output current	V_{INH} = 0 V	-15	-	-	mA
Serial peripheral interface						
input pins SDI, SCK and SCSN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pd}	pull-down resistance	on pins SCK and SDI; $V_{SCK} = V_{IL}$; $V_{SDI} = V_{IL}$	20	-	80	kΩ
R_{pu}	pull-up resistance	on pins SCK and SDI; $V_{SCK} = V_{IH}$; $V_{SDI} = V_{IH}$	20	-	80	kΩ
		on pin SCSN [4]	20	-	80	kΩ
$I_{IL(off)}$	off state input leakage current	pins SDI and SCK; Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; 0 V < V_{SDI} < V_{IO}; 0 V < V_{SCK} < V_{IO}	-5	-	+5	µA
C_i	input capacitance		-	-	10	pF
output pin SDO						
I_{OH}	HIGH-level output current	V_{SDO} = VIO - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{SDO} = 0.4 V	1	-	10	mA
$I_{OL(off)}$	off state output leakage current	$V_{SCSN} = V_{IO}$ or Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; 0 V < V_{SDO} < V_{IO}	-5	-	+5	µA
General purpose I/Os; pins GPIOx (TJA1465B only)						
I_{OH}	HIGH-level output current	$V_{GPIOx} = V_{IO}$ - 0.4 V; depending on GPIO configuration	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{GPIOx} = 0.4 V; depending on GPIO configuration	1	-	10	mA
V_{IH}	HIGH-level input voltage	depending on GPIO configuration	$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage	depending on GPIO configuration	-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage	depending on GPIO configuration	50	-	-	mV
R_{pu}	pull-up resistance	depending on GPIO configuration	20	-	80	kΩ
R_{pd}	pull-down resistance	depending on GPIO configuration	20	-	80	kΩ
$I_{OL(off)}$	off state output leakage current	high-Z or $V_{IO} < V_{uvd(VIO)}$; 0 V < V_{GPIOx} < V_{IO}	-5	-	5	µA
C_i	input capacitance	[3]	-	-	10	pF
Transmitter enable/disable input; pin TXEN_N (TJA1465B only)						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V

Table 49. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[3]	-	-	10	pF
Local wake-up input; pin WAKE						
R_{pu}	pull-up resistance	$V_{WAKE} > V_{th(wake)(max)}$ for $t > t_{wake(max)}$	100	-	400	kΩ
R_{pd}	pull-down resistance	$V_{WAKE} < V_{th(wake)(min)}$ for $t > t_{wake(max)}$	100	-	400	kΩ
$V_{th(wake)}$	wake-up threshold voltage		1.8	-	2.6	V
V_{hys}	hysteresis voltage		90	-	-	mV
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; 4.75 V ≤ V_{CC} ≤ 5.25 V				
		pin CANH; R_L = 45 Ω to 65 Ω	3	3.5	4.26	V
		pin CANL; R_L = 45 Ω to 65 Ω	0.75	1.5	2.01	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [3] [5]	0.9V_{CC}	-	1.1V_{CC}	V
$V_{cm(step)}$	common mode voltage step	[3] [5] [6]	-150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[3] [5] [6]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	CAN Active mode; dominant; Normal mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; 4.75 V ≤ V_{CC} ≤ 5.25 V [5]				
		R_L = 45 Ω to 65 Ω	1.5	-	2.75	V
		R_L = 45 Ω to 70 Ω	1.5	-	3.3	V
		R_L = 2240 Ω [3]	1.5	-	5	V
		CAN Active mode, recessive; CAN Listen-only or CAN Offline Bias mode; $V_{TXD} = V_{IO}$; no load	-50	-	+50	mV
		CAN Offline mode; no load	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	CAN Active, CAN ListenOnly or CAN Offline Bias mode; $V_{TXD} = V_{IO}$; VBATVCC = 1 or (VBATVCC = 0 and V_{BAT} ≥ 5.5 V); no load	2	2.5	3	V
		CAN Offline mode; no load	-0.1	0	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	0.5	-	0.9	V

Table 49. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		CAN Offline mode	0.4	-	1.1	V
		out-of-bounds comparator; no load; CXLDE = 1	-0.45	-	-0.25	V
$V_{rec(RX)}$	receiver recessive voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	-8	-	+0.5	V
		CAN Offline mode	-8	-	+0.4	V
		out-of-bounds comparator; no load; CXLDE = 1	-0.25	-	+9	V
$V_{dom(RX)}$	receiver dominant voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	0.9	-	9	V
		CAN Offline mode	1.1	-	9	V
		out-of-bounds comparator; no load; CXLDE = 1	-8	-	-0.45	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V; CAN Active, CAN ListenOnly or CAN Offline Bias mode; no load	50	-	-	mV
$I_{O(sc)}$	short-circuit output current	-15 V ≤ V_{CANH} ≤ +40 V; -15 V ≤ V_{CANL} ≤ +40 V	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	-27 V ≤ V_{CANH} ≤ +32 V; -27 V ≤ V_{CANL} ≤ +32 V; Normal or ListenOnly mode; V_{TXD} = V_{IO} for t > $t_{d(TXD\text{-}buspasrec)start}$[7]	-3	-	+3	mA
I_L	leakage current	V_{CC} = V_{IO} = V_{BAT} = 0 V or pins shorted to GND via 47 KΩ; V_{CANH} = V_{CANL} = 5 V	-10	-	+10	µA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	16	32	50	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	32	64	100	kΩ
C_i	input capacitance	on pins CANH, CANL to GND [3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
Signal Improvement function on CANH or CANL; +4.75 V ≤ V_{CC} ≤ +5.25 V; see Figure 14.						
$R_{i(actrec)}$	active recessive phase input resistance[8]	bus dominant-to-recessive transition; +2 V ≤ V_{CANH} ≤ V_{CC} - 2 V; +2 V ≤ V_{CANL} ≤ V_{CC} - 2 V	37.5	-	66.5	Ω
$R_{i(dif)actrec}$	active recessive phase differential input resistance[8]	$R_{i(dif)actrec}$ = $R_{i(actrec)CANH}$ + $R_{i(actrec)CANL}$	75	-	133	Ω

Table 49. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[3]	180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature	[3]	175	-	195	°C

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[3] Not tested in production; guaranteed by design.
[4] The pull-up resistance on pin SCSN is a differential resistance.
[5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in Figure 18.
[6] See Figure 11.
[7] This parameter is defined in ISO 11898-2:2024 as $t_{pas\_rec\_start}$ and is specified in the Dynamic Characteristics table (see Table 50 and Figure 14).
[8] Extended dominant and active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD.

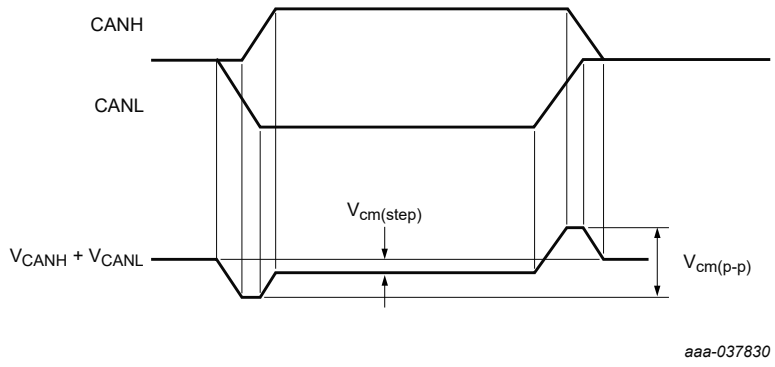


Figure 11. CAN bus common-mode voltage according to SAE 1939-14

11 Dynamic characteristics

Table 50. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN FD timing characteristics according to ISO 11898-2:2024; see Figure 12 and Figure 17						
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
CAN FD timing characteristics according to ISO 11898-2:2024; V_{CC} = 4.75 V to 5.25 V; see Figure 12, Figure 14 and Figure 17						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	80	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	80	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or ListenOnly mode	-	-	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or ListenOnly mode	-	-	110	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start	Normal mode [2] [3]	-	-	530	ns
$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start	Normal mode [2]	-	-	120	ns
$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end	Normal mode [2]	355	-	-	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)}$ ≥ 125 ns, up to 8 Mbit/s)[4]; V_{CC} = 4.75 V to 5.25 V; see Figure 12 and Figure 17						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-10	-	+10	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-20	-	+15	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-30	-	+20	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)}$ ≥ 125 ns, up to 8 Mbit/s)[4]; see Figure 12 and Figure 17						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-15	-	+15	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-25	-	+20	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-35	-	+25	ns
Dominant time-out times						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [2] [5]	0.8	-	4	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)}$ > 0.9 V; Normal or Listen Only mode [2] [5]	0.8	-	4	ms
Bus wake-up times; pins CANH and CANL; see Figure 6 and Figure 7						
$t_{wake(busdom)}$	bus dominant wake-up time	CAN Offline mode [2] [6]	0.5	-	1.45	µs

Table 50. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(busrec)}$	bus recessive wake-up time	CAN Offline mode [2] [6]	0.5	-	1.45	µs
$t_{to(wake)bus}$	bus wake-up time-out time	CAN Offline mode [2] [5]	0.8	-	9	ms
$t_{d(busact-bias)}$ [7]	bus bias reaction time	CAN Offline mode [2]	-	-	250	µs
$t_{to(silence)}$	bus silence time-out time	timer reset and restarted when bus changes from dominant to recessive or vice versa [2] [5]	0.6	-	1.2	s
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 13 [2]						
$t_{cy(clk)}$	clock cycle time	Normal, ListenOnly, Standby or Sleep mode	250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	Normal, ListenOnly, Standby or Sleep mode	50	-	-	ns
t_{SPILAG}	SPI enable lag time	Normal, ListenOnly, Standby or Sleep mode	50	-	-	ns
$t_{clk(H)}$	clock HIGH time	Normal, ListenOnly, Standby or Sleep mode	100	-	-	ns
$t_{clk(L)}$	clock LOW time	Normal, ListenOnly, Standby or Sleep mode	100	-	-	ns
$t_{r(clk)}$	clock rise time	Normal, ListenOnly, Standby or Sleep mode; 10 % to 90 %	-	-	20	ns
$t_{f(clk)}$	clock fall time	Normal, ListenOnly, Standby or Sleep mode; 90 % to 10 %	-	-	20	ns
$t_{su(D)}$	data input set-up time	Normal, ListenOnly, Standby or Sleep mode	50	-	-	ns
$t_{h(D)}$	data input hold time	Normal, ListenOnly, Standby or Sleep mode	50	-	-	ns
$t_{v(Q)}$	data output valid time	C_L = 30 pF; Normal, ListenOnly, Standby or Sleep mode; pin SDO	-	-	50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	C_L = 30 pF; Normal, ListenOnly, Standby or Sleep mode; SPI address bits and read-only bit; pin SDO	-	-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH	Normal, ListenOnly, Standby or Sleep mode	250	-	-	ns
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW	Normal, ListenOnly, Standby or Sleep mode; pin SCSN	50	-	-	ns
$t_{to(SPI)}$ [8]	SPI time-out time	[5]	1.6	-	2.4	ms

Table 50. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN partial networking						
$N_{bit(idle)}$[7]	number of idle bits	before a SOF is accepted [2]	6	-	10	-
$t_{fltr(bit)dom}$	dominant bit filter time	arbitration bit rate ≤ 500 kbit/s; IDFS = 0x0 [2] [9]	5	-	17.5	%
		ISO bitfilter 1; IDFS = 0x1 [2] [9]	5	-	17.5	%
		ISO bitfilter 2; IDFS = 0x2 [2]	2.5	-	8.75	%
		IDFS = 0x3 [2]	18	-	93	ns
		IDFS = 0x4 [2]	42	-	119	ns
		IDFS = 0x5 [2]	67	-	145	ns
		IDFS = 0x6 [2]	91	-	170	ns
General purpose I/Os; pins GPIOx (TJA1465B only)						
t_{fltr}	filter time	pin configured as input except for GPIOxFS = 0x03 (TXEN_N input) and GPIO2FS = 0x05 or 0x07 (TXD2 input) [10]	1	-	21	µs
		pin configured as TXEN_N input with GPIOxFS = 0x03 [10]	1	-	5	µs
$t_{w(min)}$	minimum pulse width	pin configured as output except when RXD2 option is selected for GPIO1 [2]	3	-	-	µs
Transmitter enable/disable input; pin TXEN_N (TJA1465B only)						
t_{fltr}	filter time	[10]	1	-	5	µs
Mode transitions; see Section 7.2, Figure 6 and Figure 7						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	µs
$t_{startup}$	start-up time	[2]	-	-	1	ms
$t_{startup(RXD)}$	RXD start-up time	after local or remote wake-up detected [2] [11]	0	-	20	µs
$t_{startup(INH)}$	INH start-up time	after local or remote wake-up detected; transition from Sleep to Standby [2] [12]	0	-	40	µs
$t_{t(snm)}$	SNM transition time	bus dominant time for Start-to-Normal mode boot [2] [13]	11	-	16	ms
$t_{to(MCU)}$	MCU time-out time	(1): LUVIOSEL = 0; $t_{to(MCU)1}$ [2]	825	-	1300	ms
		(2): LUVIOSEL = 1; $t_{to(MCU)2}$ [2]	1650	-	2600	ms
Local wake-up input; pin WAKE, see Section 7.2.2 and Table 36						
t_{wake}	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode [14]				

Table 50. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		short wake-up time: WFC = 0 [2]	20	-	50	µs
		long wake-up time: WFC = 1 [2]	12	-	18	ms
Undervoltage detection; see Table 8 and Table 12[2]						
$t_{det(uv)}$	undervoltage detection time	≥ 100 mV input overdrive				
		on pin VBAT	-	-	30	µs
		on pin VCC	-	-	36	µs
		on pin VIO	-	-	36	µs
$t_{det(uv)long}$	long undervoltage detection time	on pin VIO; LUVIOSEL = 0; $t_{det(uv)long1}$ [15]	100	-	160	ms
		on pin VIO; LUVIOSEL = 1; $t_{det(uv)long2}$ [15]	850	-	1150	ms
$t_{rec(uv)}$	undervoltage recovery time	≥ 100 mV input overdrive				
		on pin VBAT	-	-	50	µs
		on pin VCC	-	-	56	µs
		on pin VIO	-	-	46	µs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] If TXD goes LOW before the recessive transition has been completed, the bus switches to dominant.
[4] Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s) and B ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbit/s).
[5] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
[6] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
[7] As specified in ISO 11898-2:2024.
[8] See Section 7.10.1'
[9] Up to 2 Mbit/s data bit rate.
[10] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.
[11] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 6 and Figure 7.
[12] INH switches HIGH between the min and max values after a wake-up had been detected. INH is guaranteed to be floating below the min value and guaranteed to be HIGH above the max value; see Figure 6 and Figure 7.
[13] The transition occurs between the min and max times. The transition is guaranteed not to occur below the min value; the transition is guaranteed to occur above the max value.
[14] Wake-up occurs between min and max values. Wake-up is guaranteed not to occur below the min value; wake-up is guaranteed to occur above the max value.
[15] An undervoltage longer than the max value is guaranteed to force a transition to Sleep mode; an undervoltage shorter than the min value is guaranteed not to force a transition to Sleep mode.

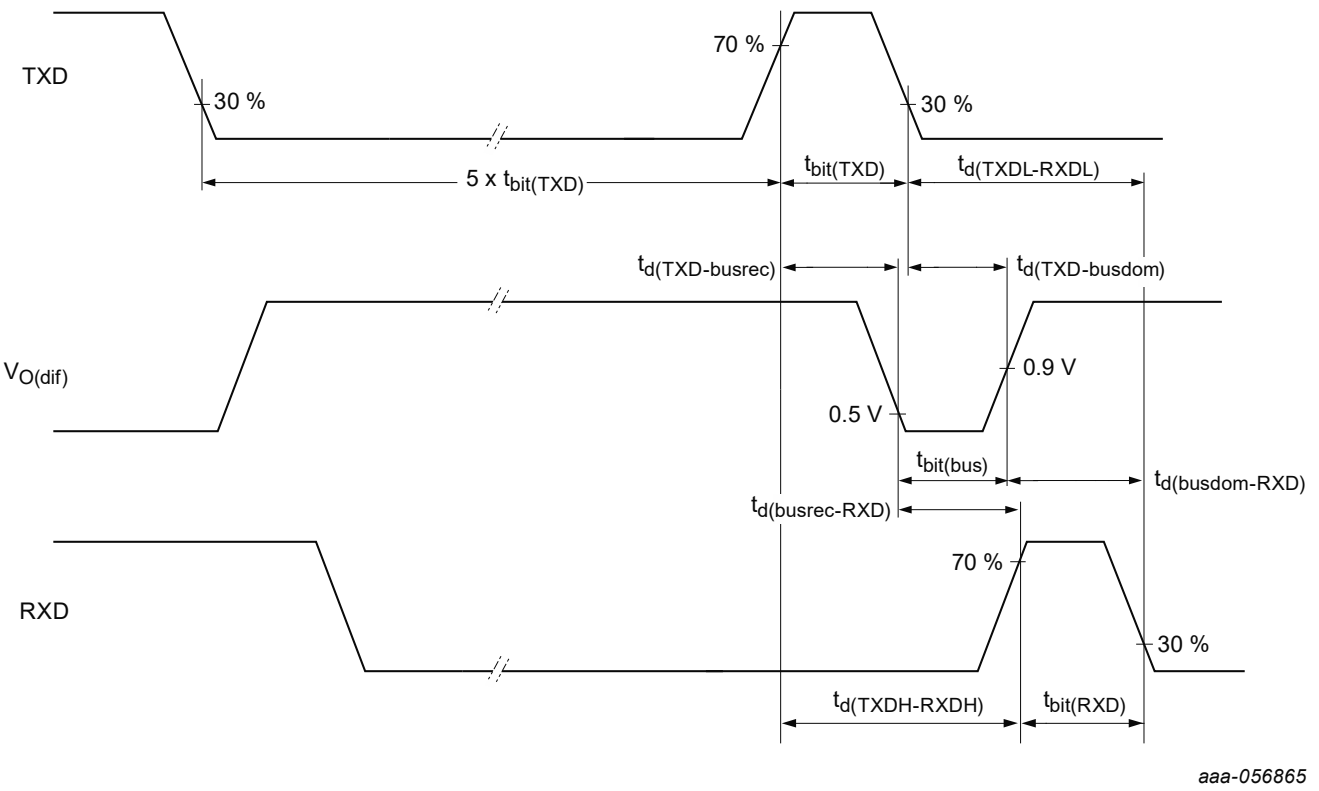
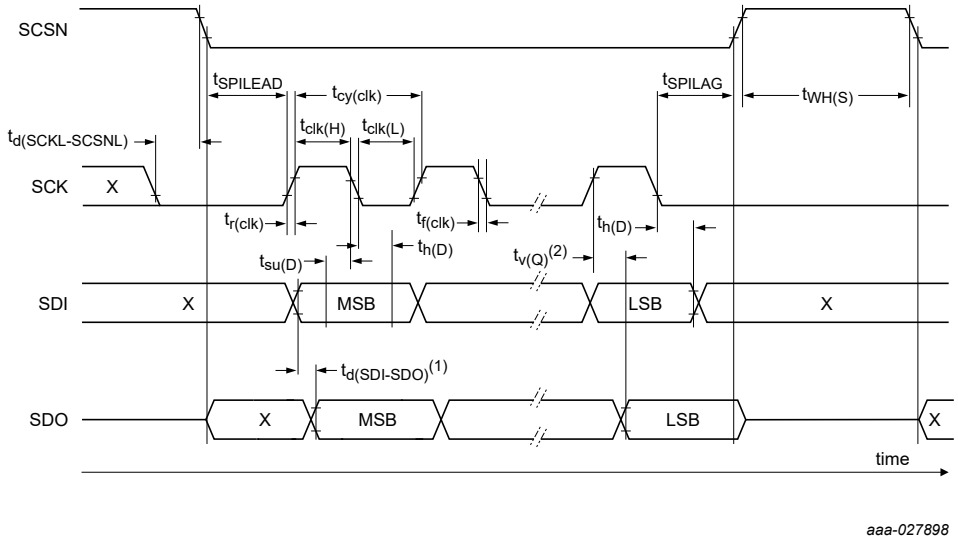


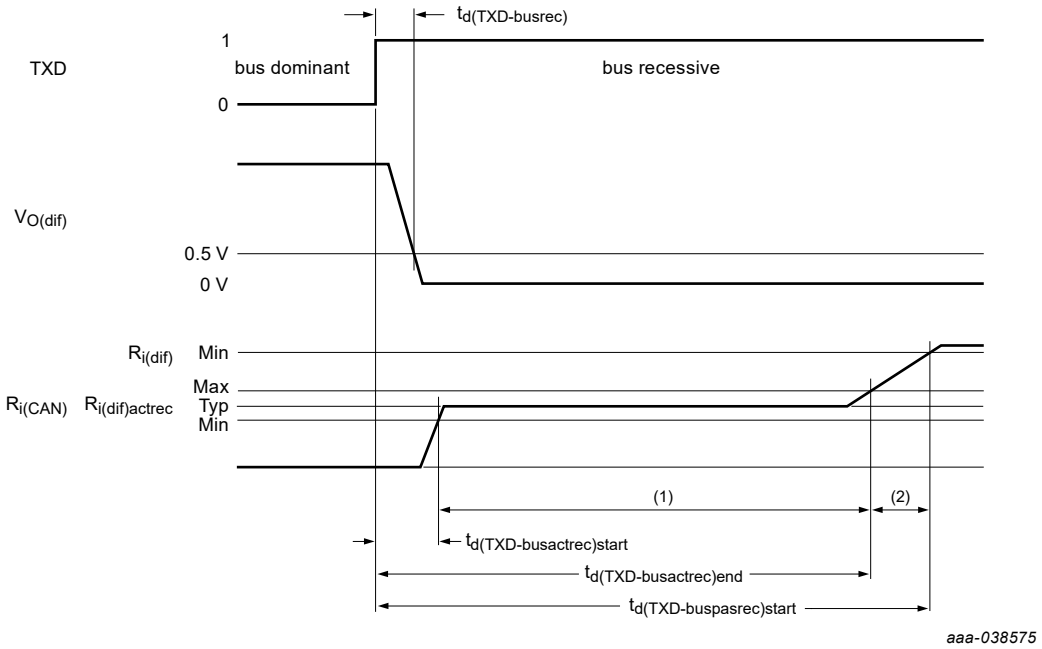
Figure 12. CAN transceiver timing diagram according to ISO 11898-2:2024



(1) The SDI to SDO delay time is valid for SPI address bits and the read-only bit.

(2) The data output valid time is valid for the SPI data bits.

Figure 13. SPI timing diagram



(1) Active recessive phase (2) Slow release phase.

Figure 14. TJA1465 transmitter impedance and timing diagram for dominant-to-passive recessive transition according to ISO 11898-2:2024 parameter set C

12 Application information

Example 12 V applications with components typically used with the TJA1465 are shown in Figure 15 and Figure 16. See the application hints (Section 12.2) for further information about external components and PCB layout requirements.

12.1 Application diagram

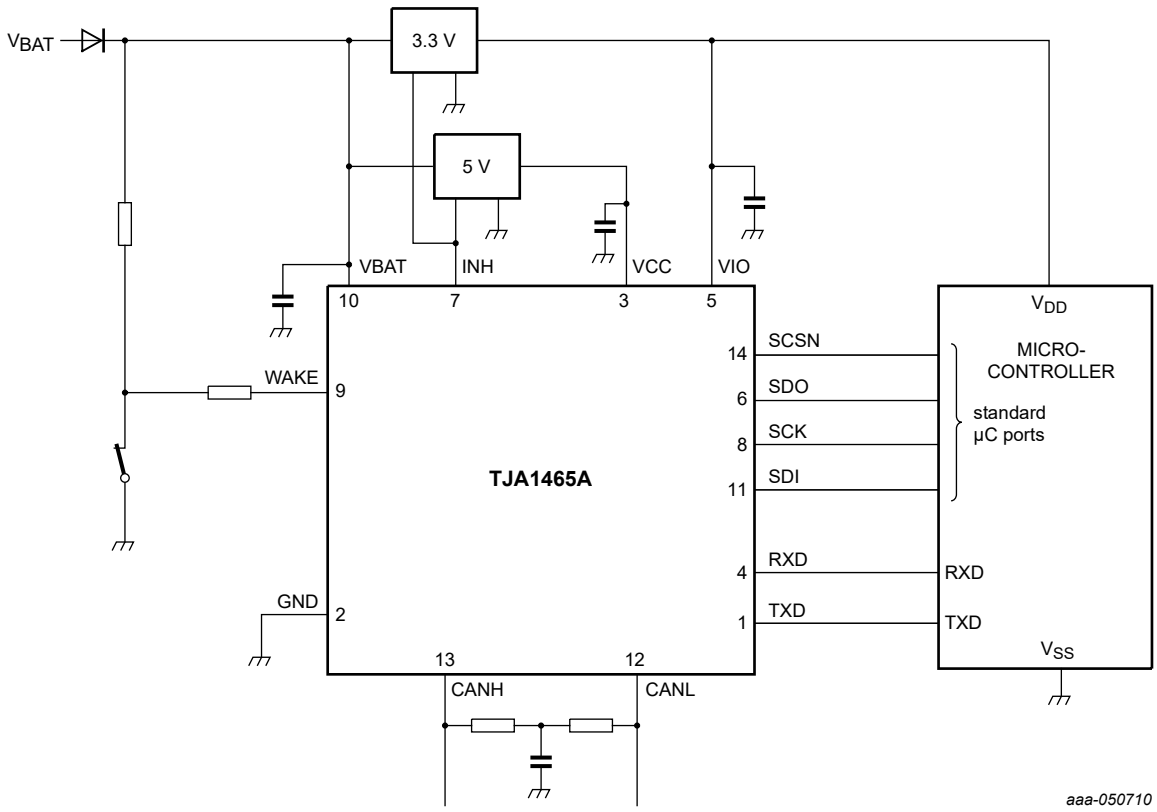


Figure 15. Typical TJA1465A application with a 3.3 V microcontroller

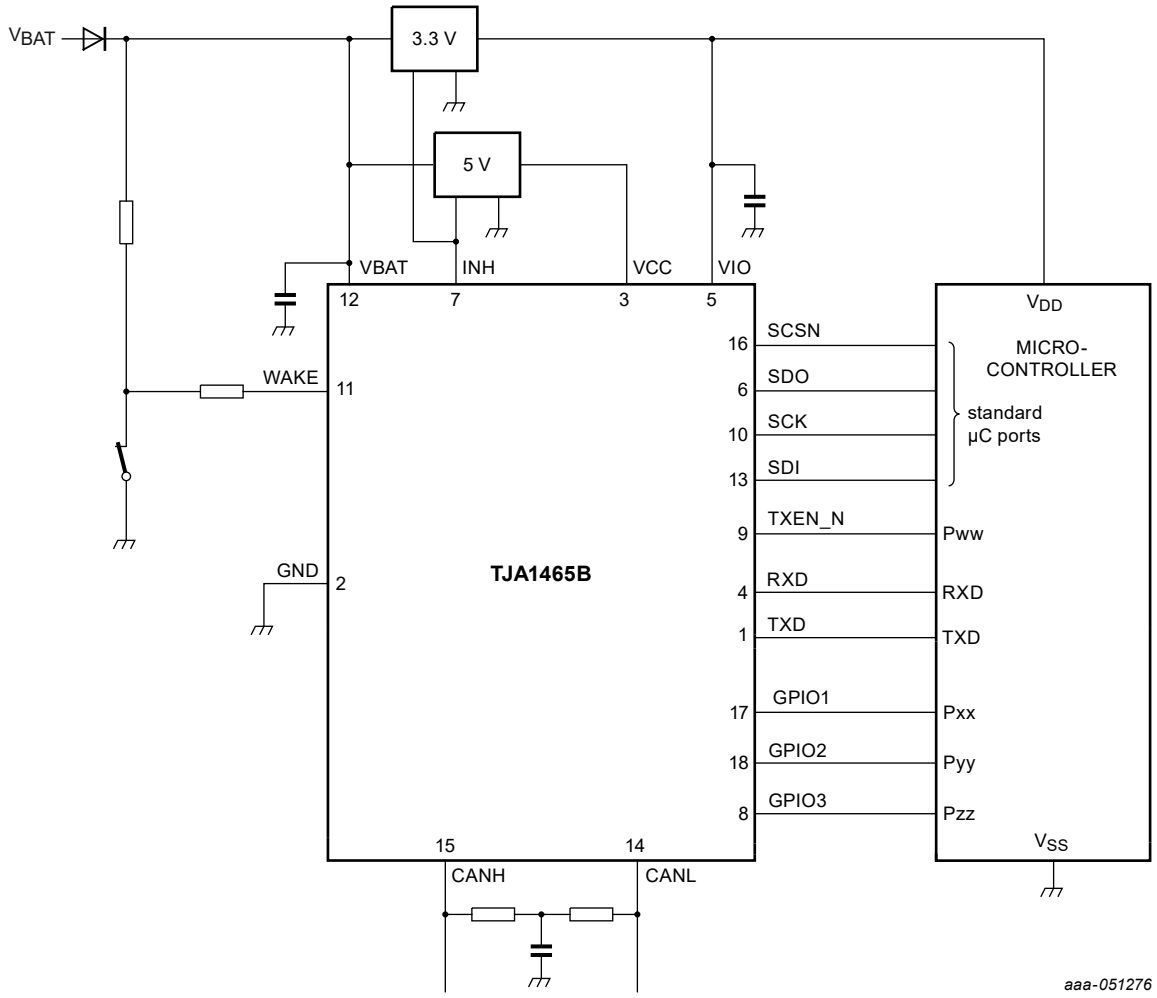


Figure 16. Typical TJA1465B application with a 3.3 V microcontroller

12.2 Application notes

Further information on the application of the TJA1465 can be found in NXP application notes AN14338 '*TJA1445, TJA1465 application note*', available on request from NXP Semiconductors.

13 Test information

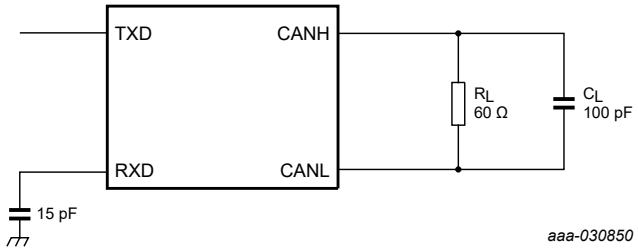


Figure 17. CAN transceiver timing test circuit

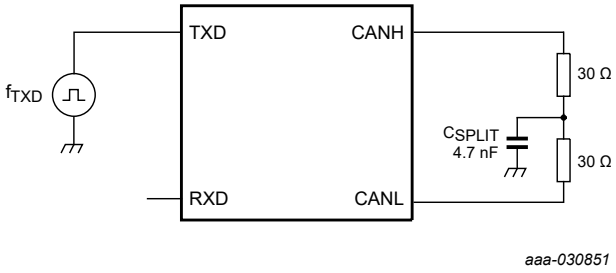


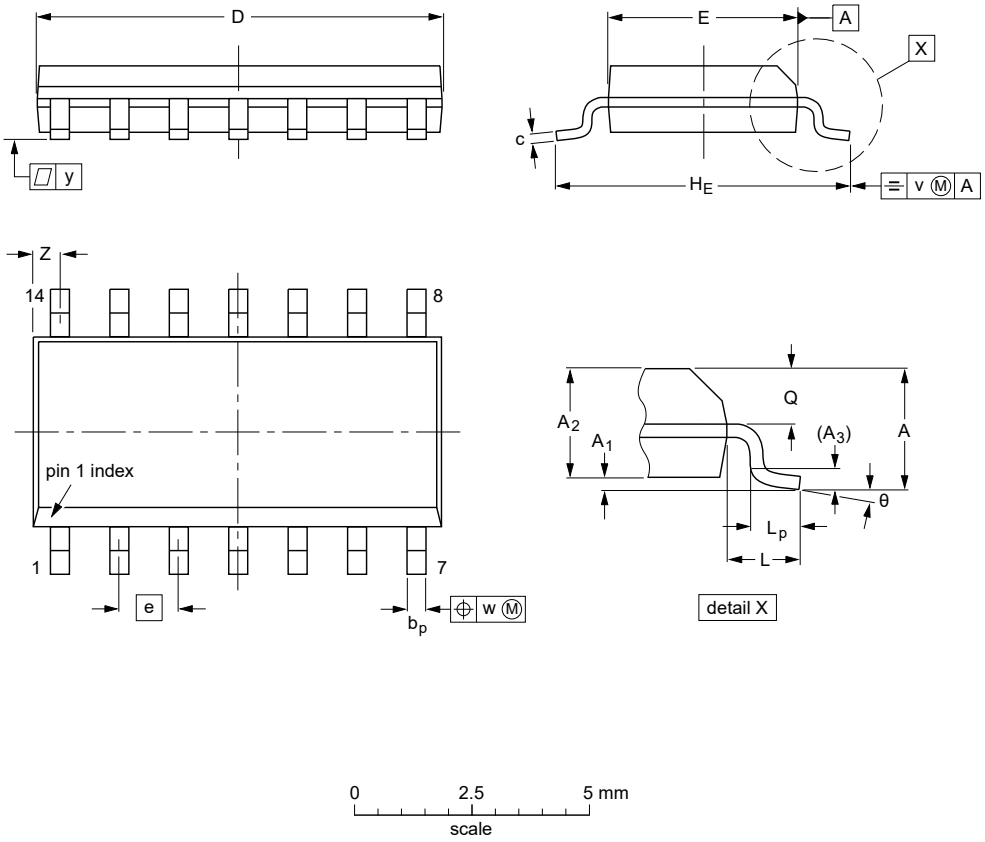
Figure 18. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

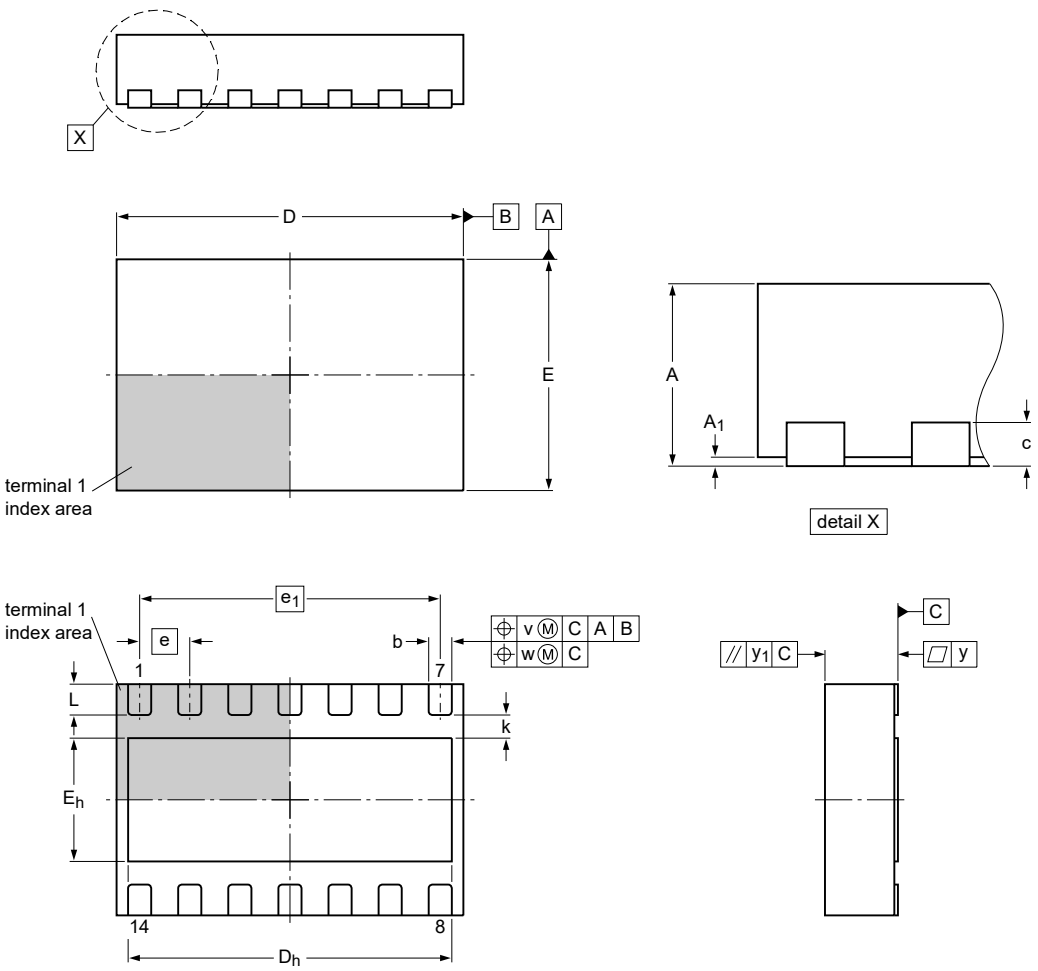
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 19. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit	A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

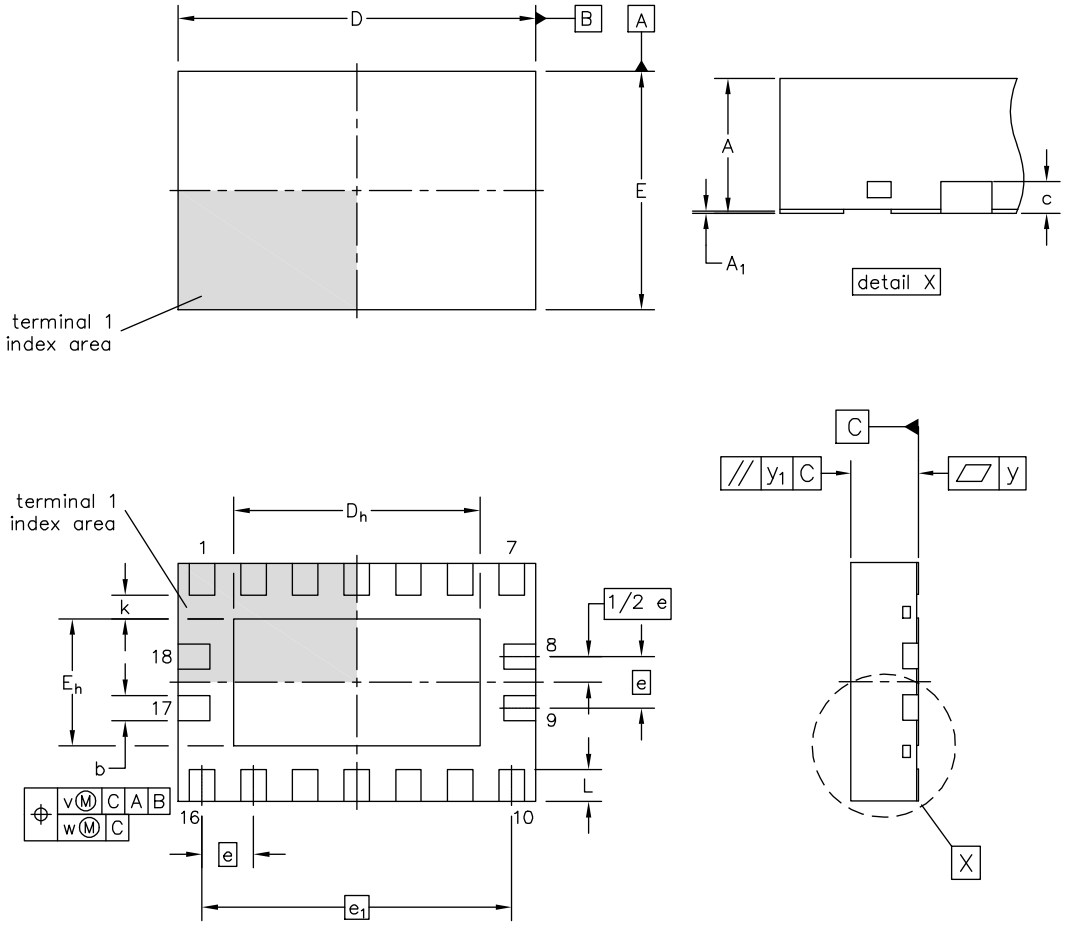
sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 20. Package outline SOT1086-2 (HVSON14)

DHVQFN18: plastic dual in−line compatible thermal enhanced very thin quad flat package; no leads; 18 terminals; body 3.0 x 4.5 x 0.85 mm

SOT2163−1



DIMENSIONS (mm are the original dimensions)

Unit[1]	A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
max	1.00	0.05	0.35		4.60	3.15	3.10	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.20	4.50	3.10	3.00	1.60	0.65	3.90	0.30	0.40	0.10	0.05	0.05	0.10
min	0.80	0.00	0.29		4.40	3.05	2.90	1.55			0.25	0.35				

Note

1.Plastic or metal protusions of 0.075 mm maximum per side are not included.

DATE: 06 DEC 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01851D	REVISION: 0	

Figure 21. Package outline SOT2163-1 (DHVQFN18)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 51 and Table 52

Table 51. SnPb eutectic process (from J-STD-020D)

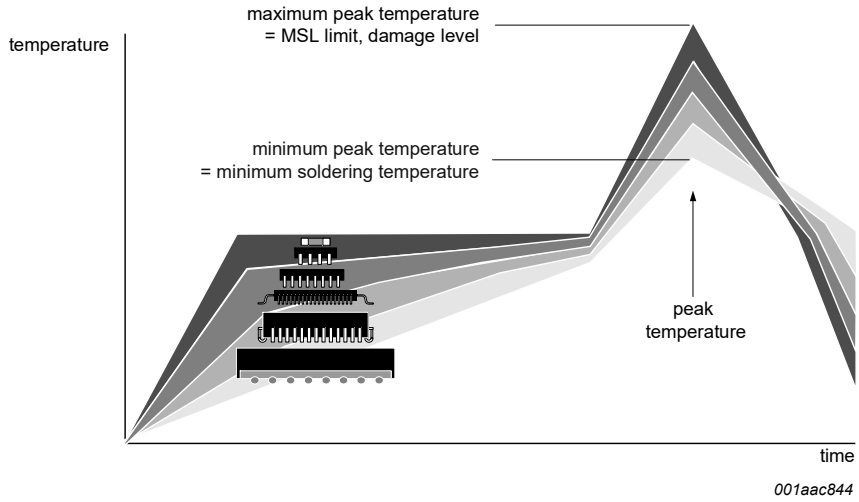
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 52. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Figure 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Appendix: ISO 11898-2:2024 parameter cross-reference lists

Table 53. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	$R_{DIFF\_pas\_rec}$	$R_{i(dif)}$	differential input resistance
Single-ended internal resistance	$R_{SE\_pas\_rec\_H}$ $R_{SE\_pas\_rec\_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry			
Driver symmetry	V_{sym_vcc}	V_{TXsym}	transmitter voltage symmetry
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time

Table 53. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]*...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA implementation loop delay requirements for parameter sets A, B and C			
Loop delay for parameter sets A and B	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
Loop delay for parameter set C		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD\_BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS\_RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominent to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter sets A, B and C			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C			
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF\_act\_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Internal single-ended resistance	$R_{SE\_act\_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Start time of active signal improvement phase	$t_{act\_rec\_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act\_rec\_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas\_rec\_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start
PMA voltage wake-up control timing			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH)}$	INH start-up time
		$t_{startup(ERR\_N)}$	ERR_N start-up time
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits before a SOF is accepted
BitFilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter\_option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter\_option2}$		
HS-PMA bus biasing control timing			
Time-out for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	bus bias reaction time

[1] A number of proprietary NXP parameters are equivalent to parameters defined in ISO 11898-2:2024, but use different symbols. This conversion table allows ISO parameters to be cross-referenced with their NXP counterparts. The NXP parameters are defined in the Static and Dynamic characteristics tables. The conversion table provides a comprehensive listing - individual devices may not include all parameters.

18 Appendix: TJA1445x/TJA1446x/TJA1465x/TJA1466x family overview

Table 54. Feature overview of the the complete TJA1445x/TJA1446x/TJA1465x/TJA1466x family.

	Partial Networking			V_{IO} supply			Data rate		Special features							
Device	Selective wake-up	CAN FD passive	CAN XL passive	1.8 V V_{IO}	3.3 V V_{IO}	5.0 V V_{IO}	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN SIC	ISO 26262 ASIL B compliance	GPIO pins	TXEN_N pin	RST_N pin	FSO/LIMP pin	V_{IO} undervoltage monitoring	V_{IO} overvoltage monitoring	Q&A watchdog
TJA1445A	●	●		●	●	●	●		●					●		
TJA1445B	●	●		●	●	●	●		●	3	●			●		
TJA1446A	●	●		●			●		●	2		●	●	●	●	●
TJA1446B	●	●			●		●		●	2		●	●	●	●	●
TJA1446C	●	●				●	●		●	2		●	●	●	●	●
TJA1465A	●	●	●	●	●	●	●	●	●					●		
TJA1465B	●	●	●	●	●	●	●	●	●	3	●			●		
TJA1466A	●	●	●	●			●	●	●	2		●	●	●	●	●
TJA1466B	●	●	●		●		●	●	●	2		●	●	●	●	●
TJA1466C	●	●	●			●	●	●	●	2		●	●	●	●	●

19 Revision history

Table 55. Revision history

Document ID	Release date	Description
TJA1465 v.1.0	16 October 2024	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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